

Fig. 1
Prior Art

00000767 113001

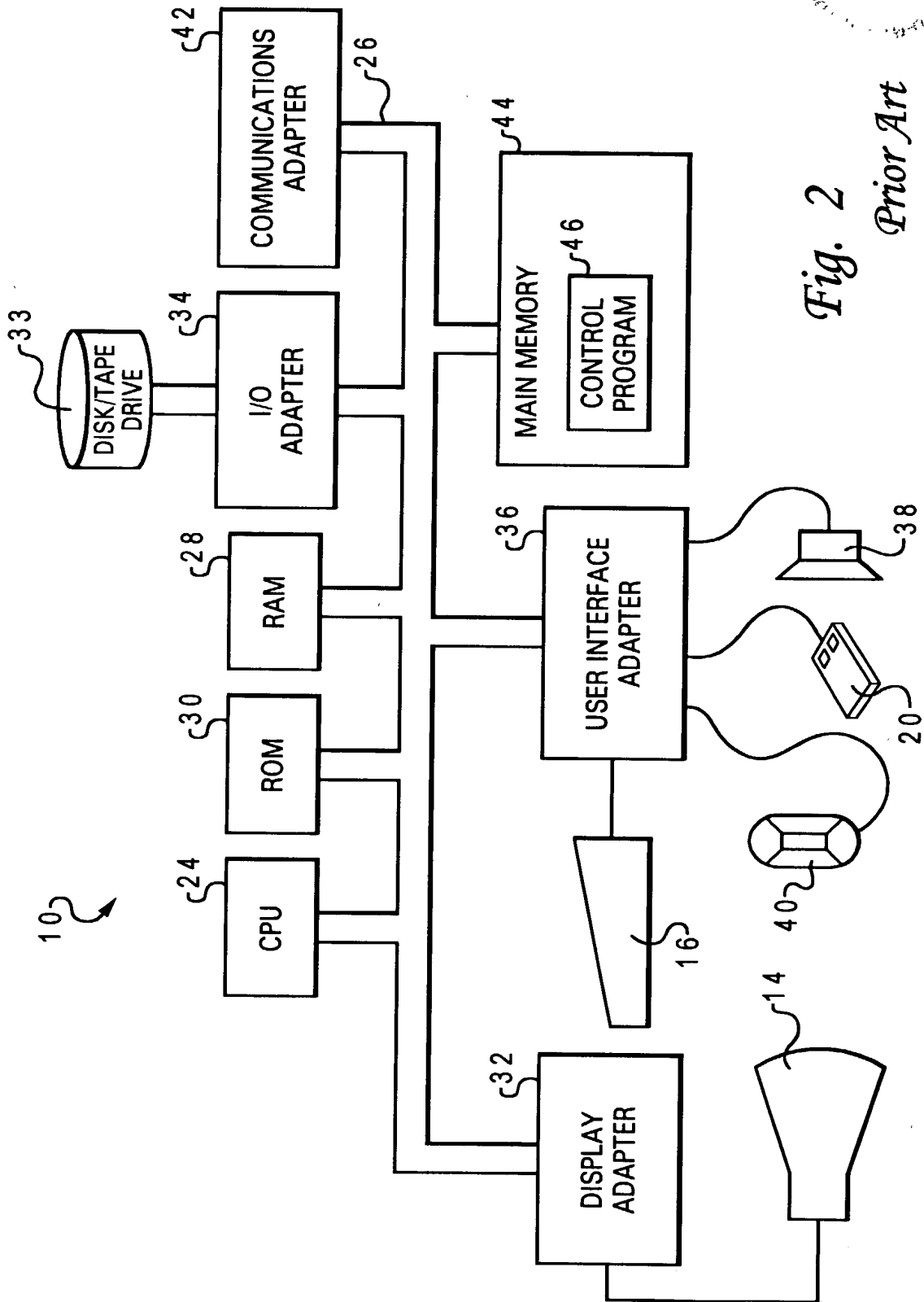


Fig. 2
Prior Art

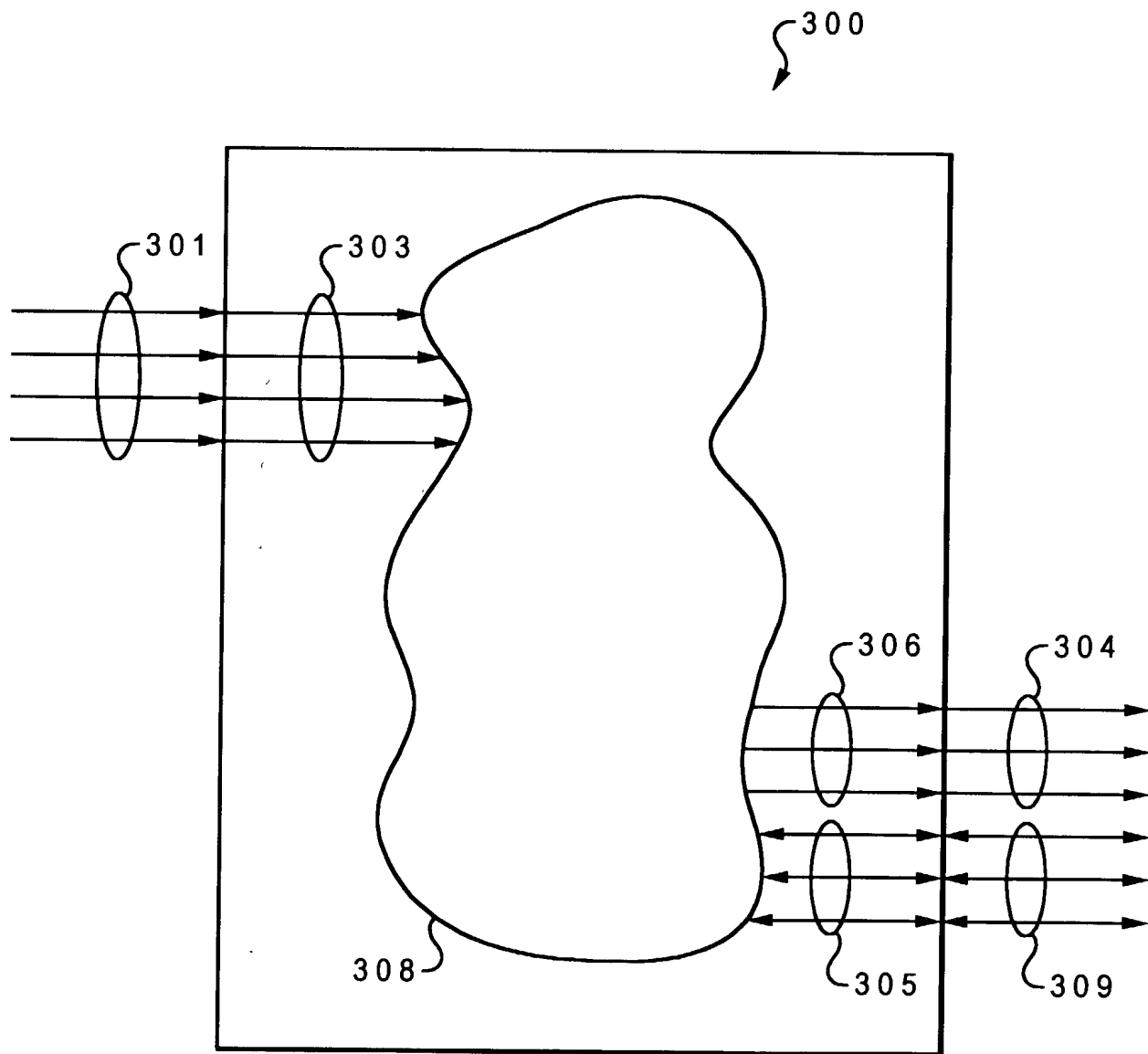


Fig. 3A

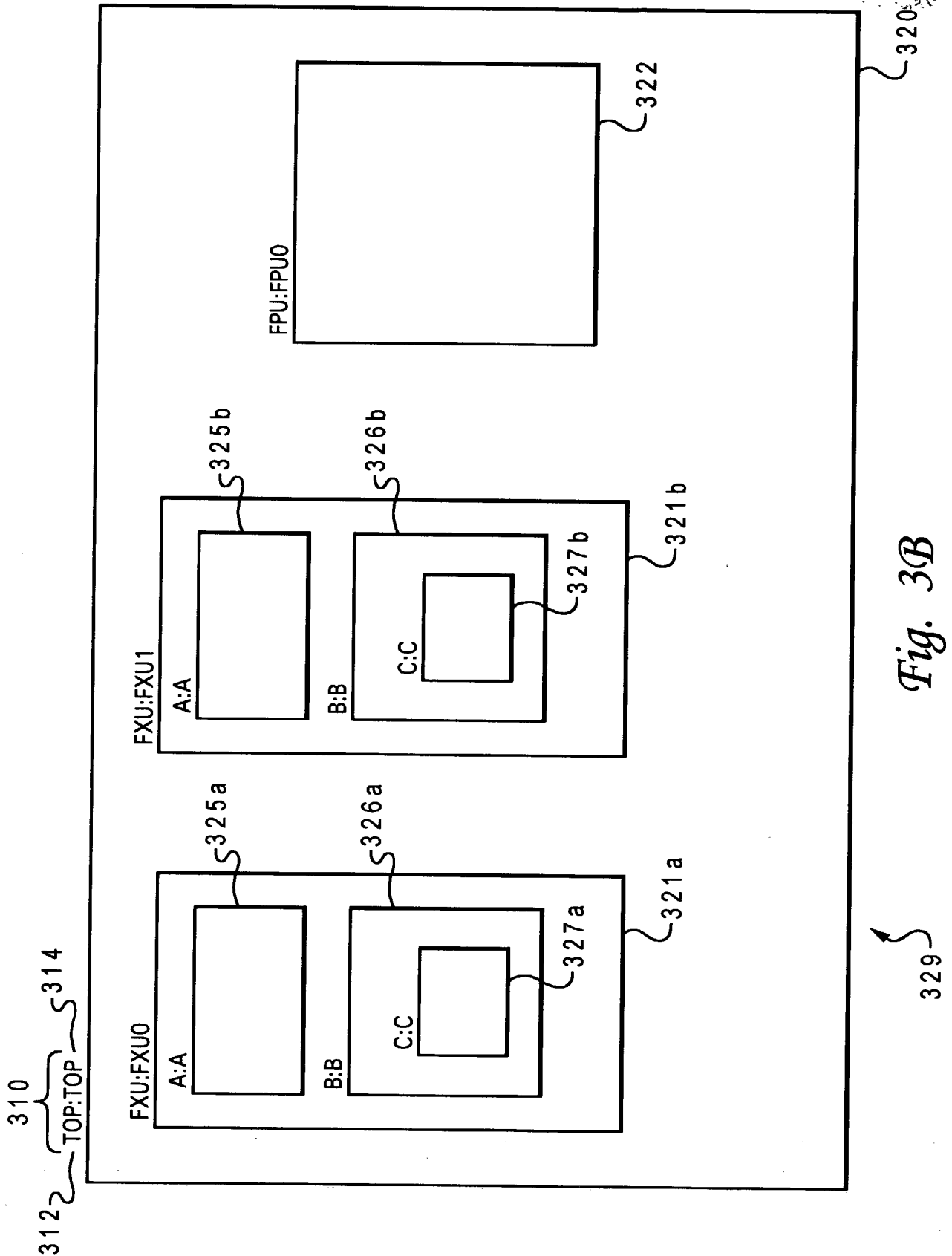


Fig. 3B

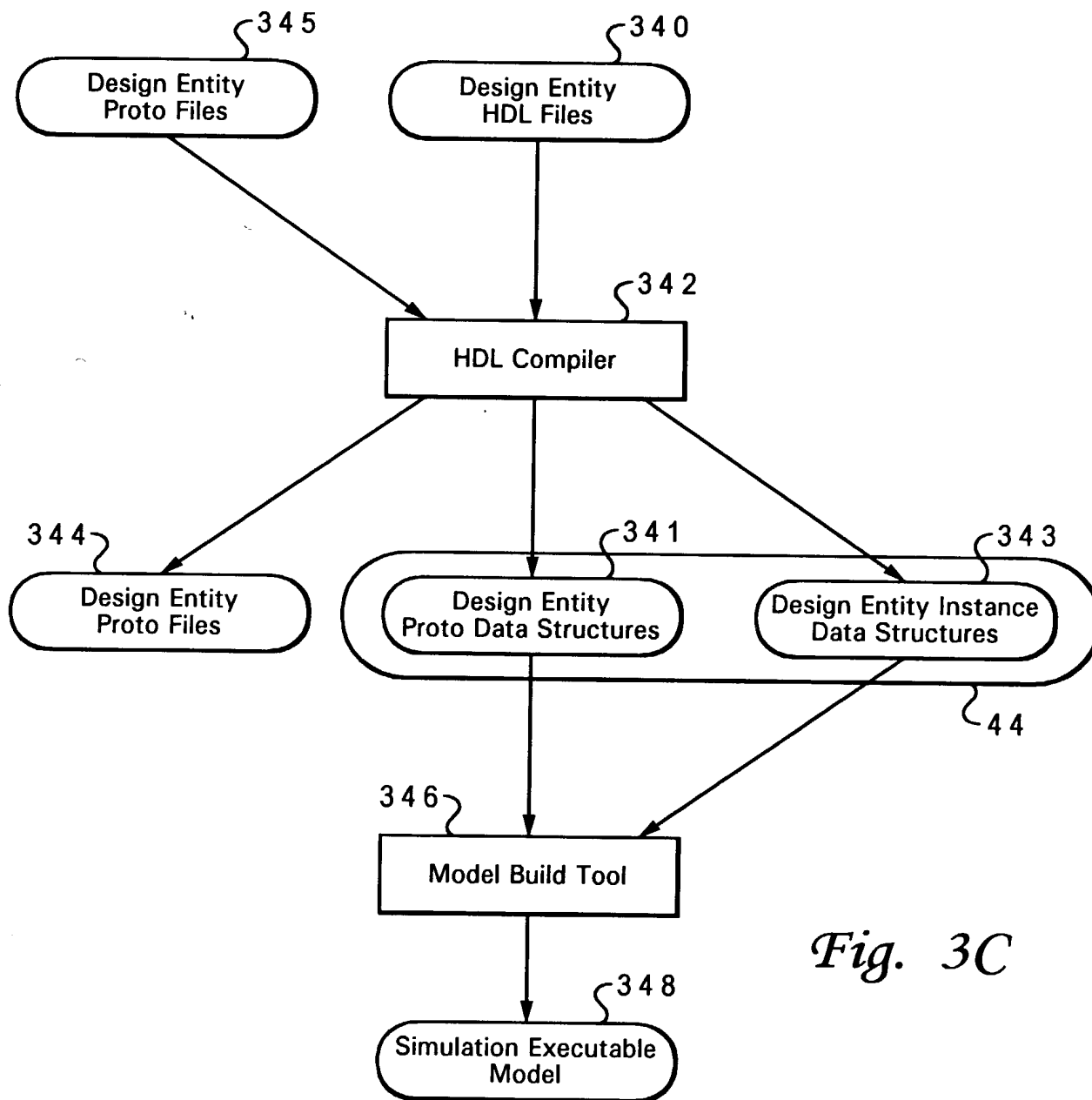


Fig. 3C

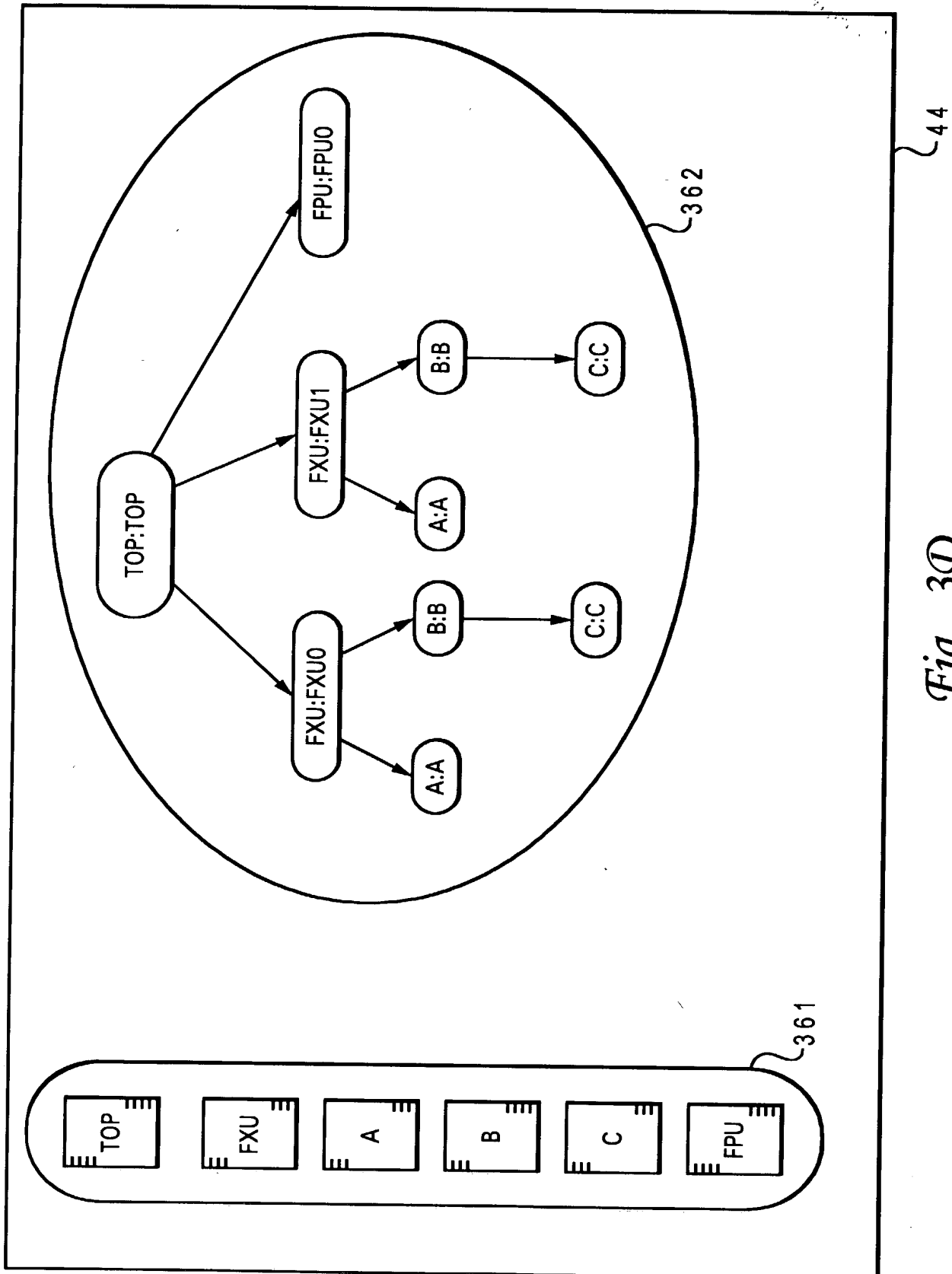


Fig. 3D

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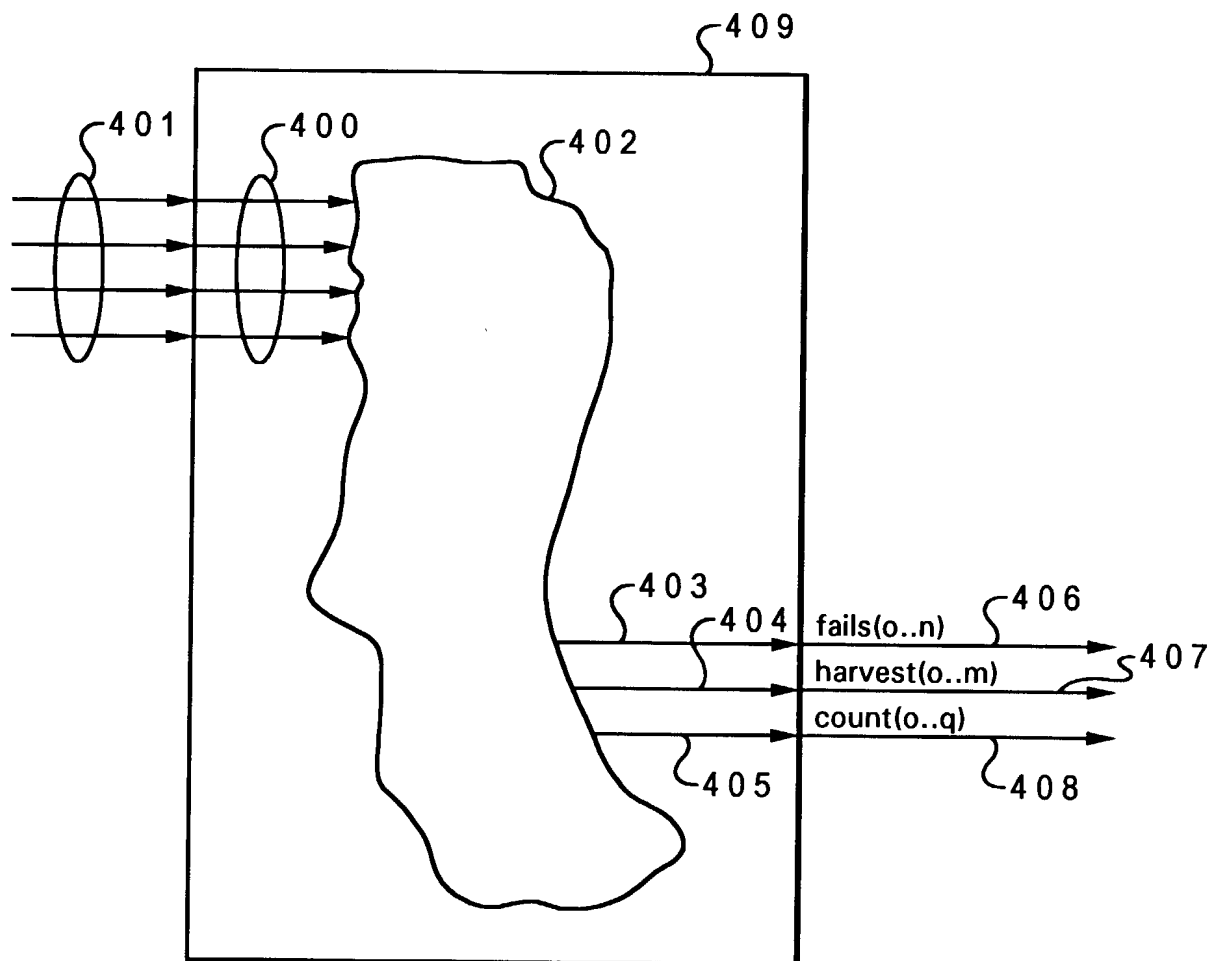


Fig. 4A

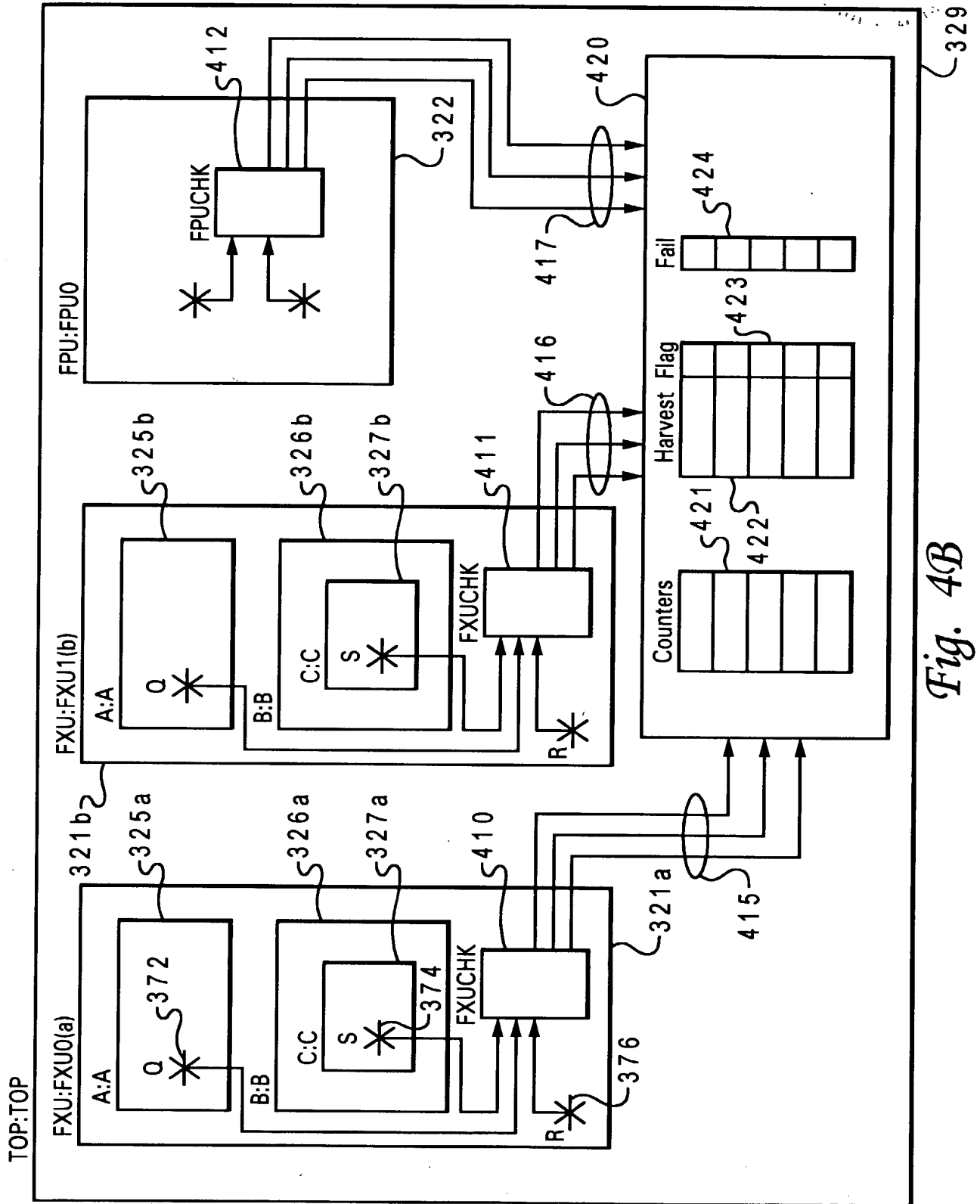


Fig. 4B

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ENTITY FXUCHK IS

```

PORT(
    S_IN      :    IN std_ulogic;
    Q_IN      :    IN std_ulogic;
    R_IN      :    IN std_ulogic;
    clock      :    IN std_ulogic;
    fails      :    OUT std_ulogic_vector(0 to 1);
    counts     :    OUT std_ulogic_vector(0 to 2);
    harvests   :    OUT std_ulogic_vector(0 to 1);
);

```

- 4 5 0

```
4 5 2 { --!! BEGIN
        --!! Design Entity: FXU;
```

```

4 5 3 { --!! Inputs
      --!! S_IN      => B.C.S;
      --!! Q_IN      => A.Q;
      --!! R_IN      => R;
      --!! CLOCK      => clock;
      --!! End Inputs

```

```
4 5 4 { --!! Fail Outputs;  
      --!! 0 : "Fail message for failure event 0";  
      --!! 1 : "Fail message for failure event 1";  
      --!! End Fail Outputs;
```

- 4 5 1

```

4 5 5 { --!! Count Outputs;
        --!! 0 : <event0> clock;
        --!! 1 : <event1> clock;
        --!! 2 : <event2> clock;
        --!! End Count Outputs;

```

```
4 5 6 { --!! Harvest Outputs;  
      --!! 0 : "Message for harvest event 0";  
      --!! 1 : "Message for harvest event 1";  
      --!! End Harvest Outputs;
```

4 5 7 { --!! End;

ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

- 4 5 8

END;

- 440

Fig. 4C

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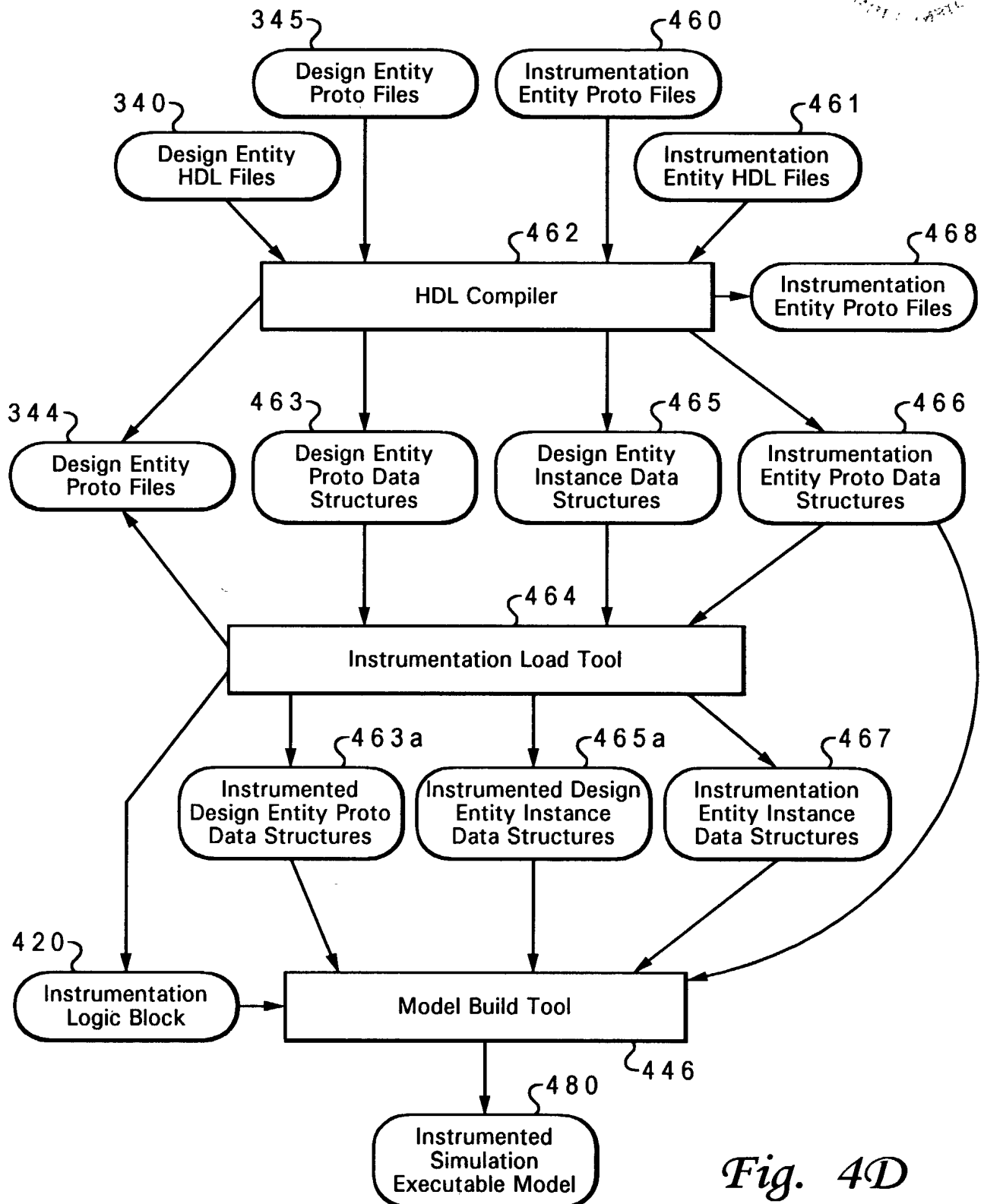


Fig. 4D

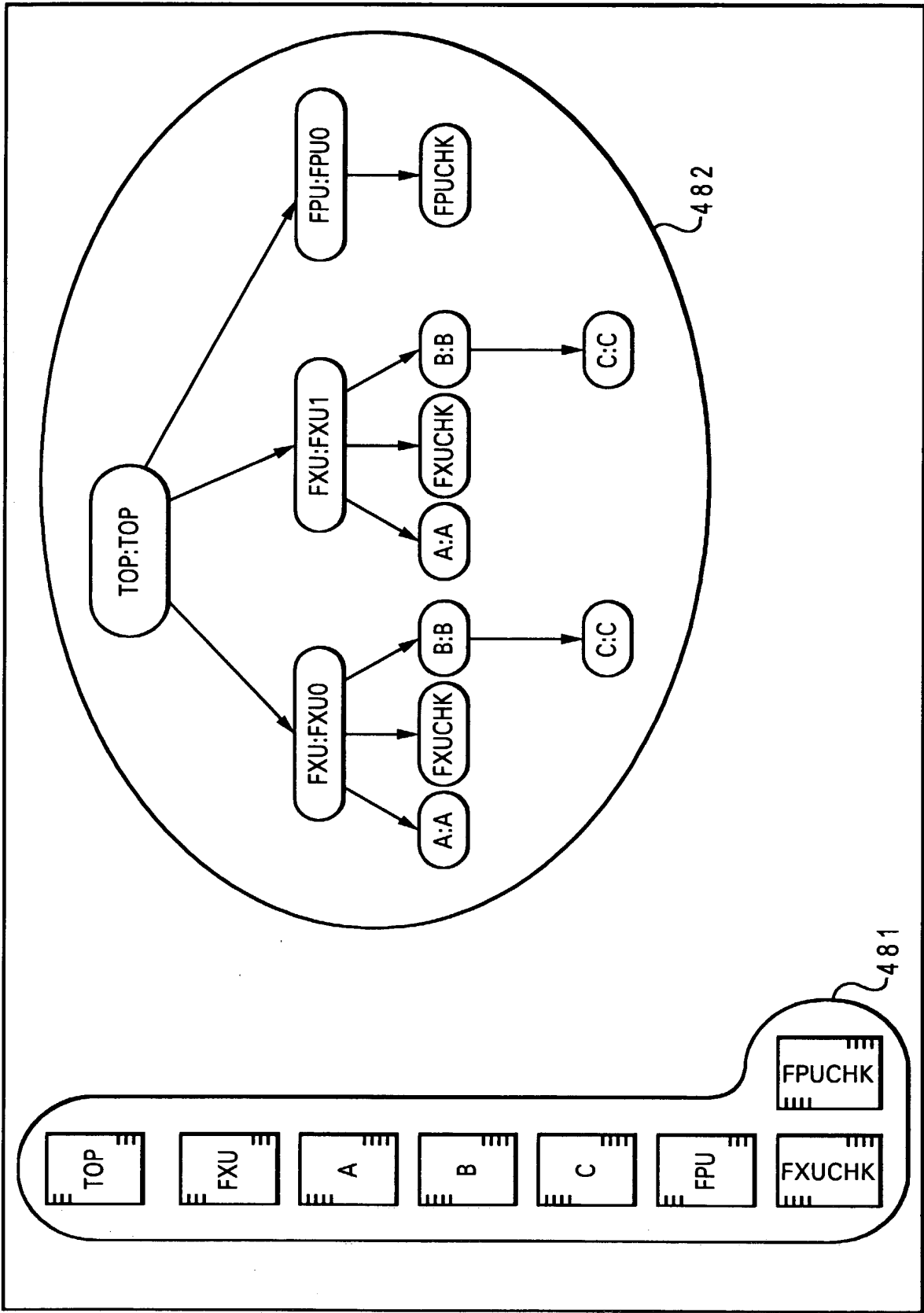


Fig. 4E

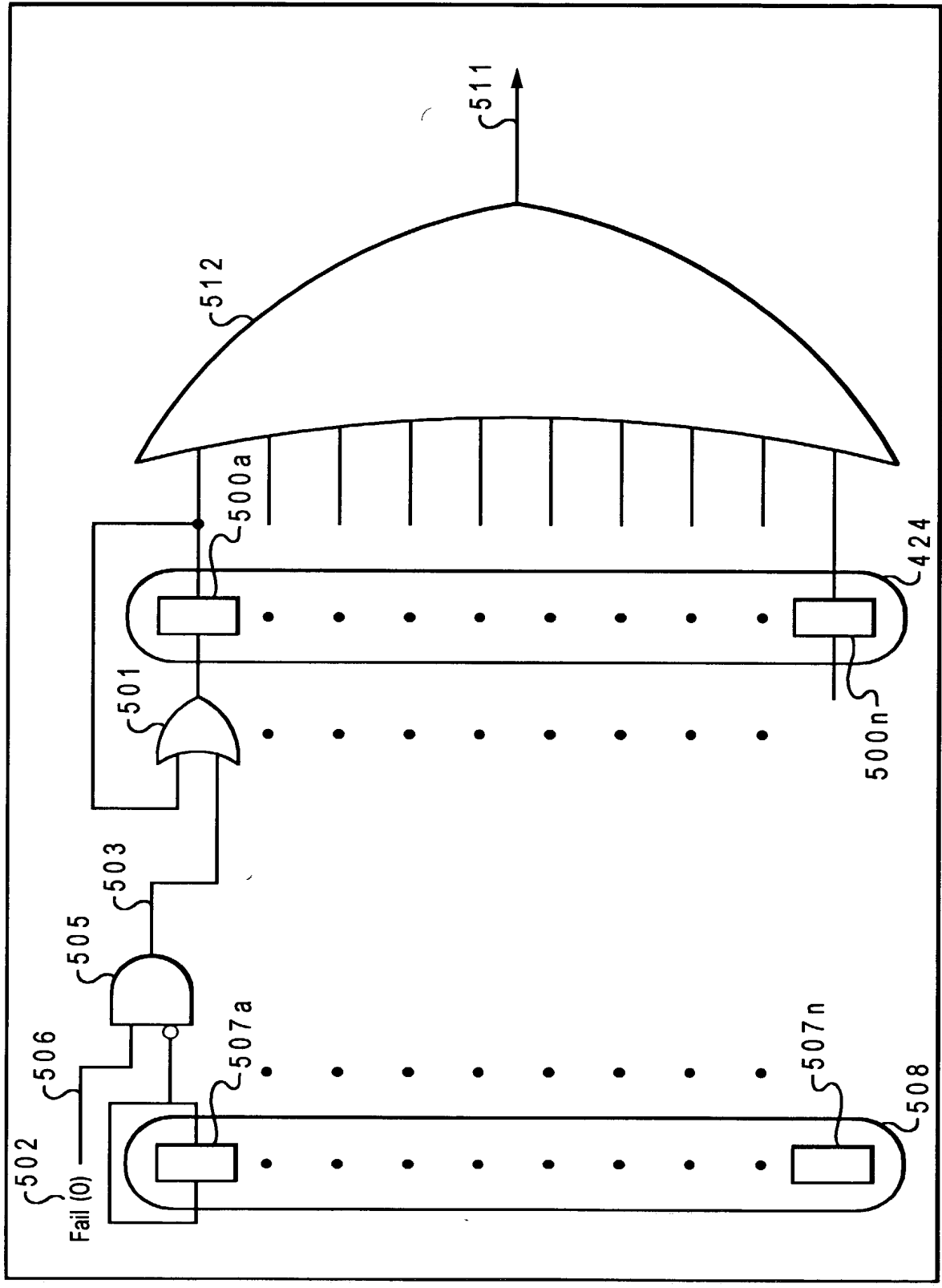


Fig. 5A

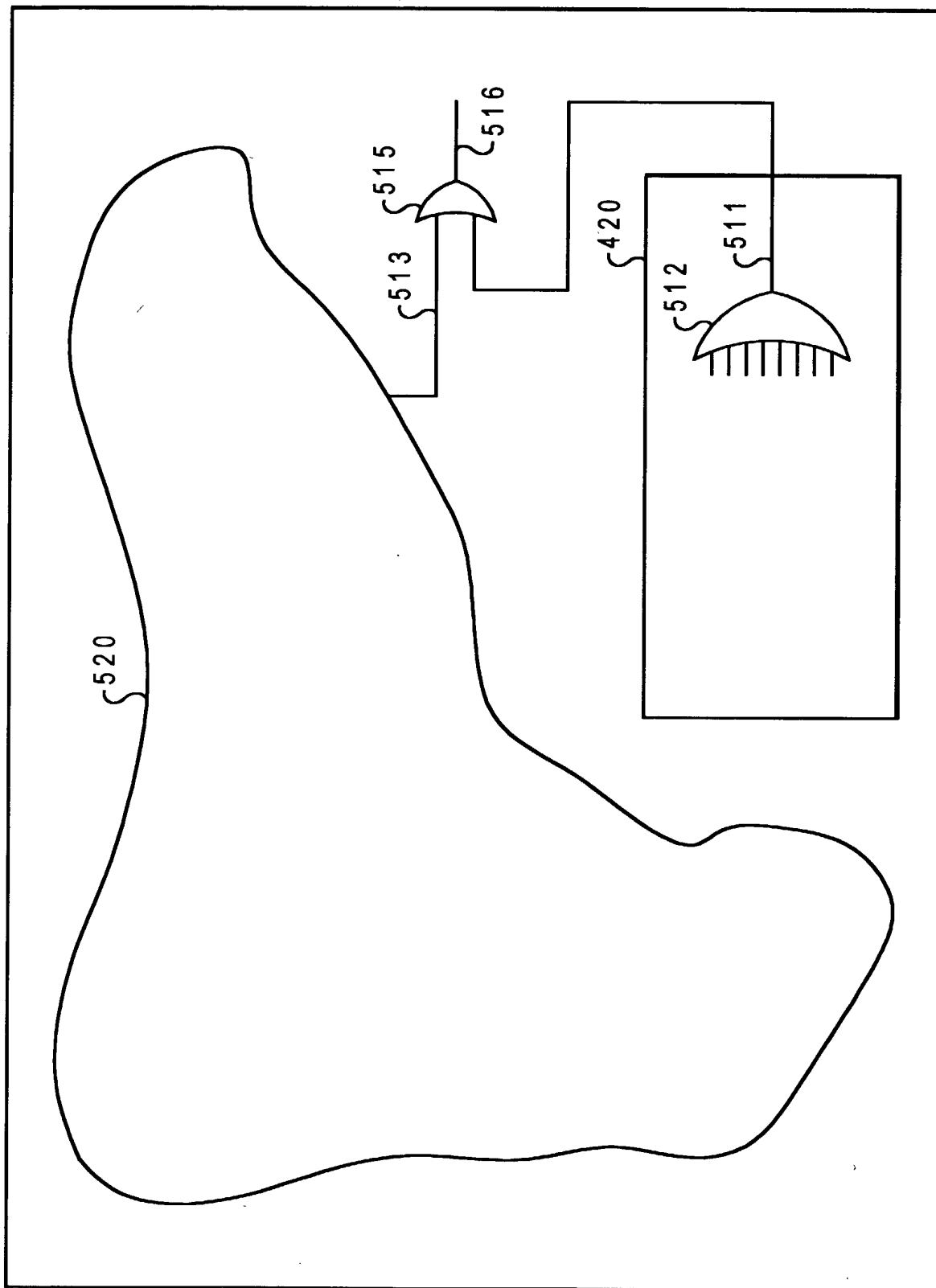


Fig. 5B

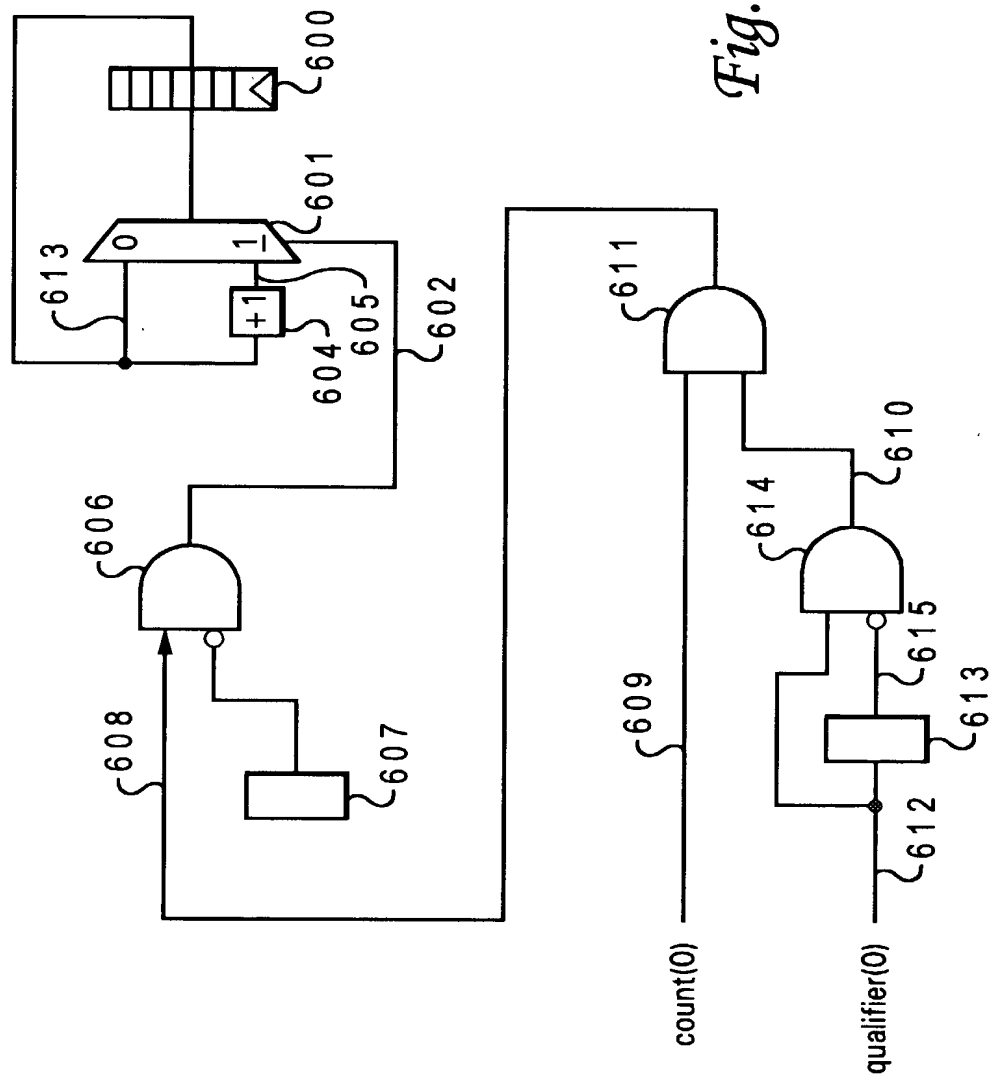


Fig. 6A

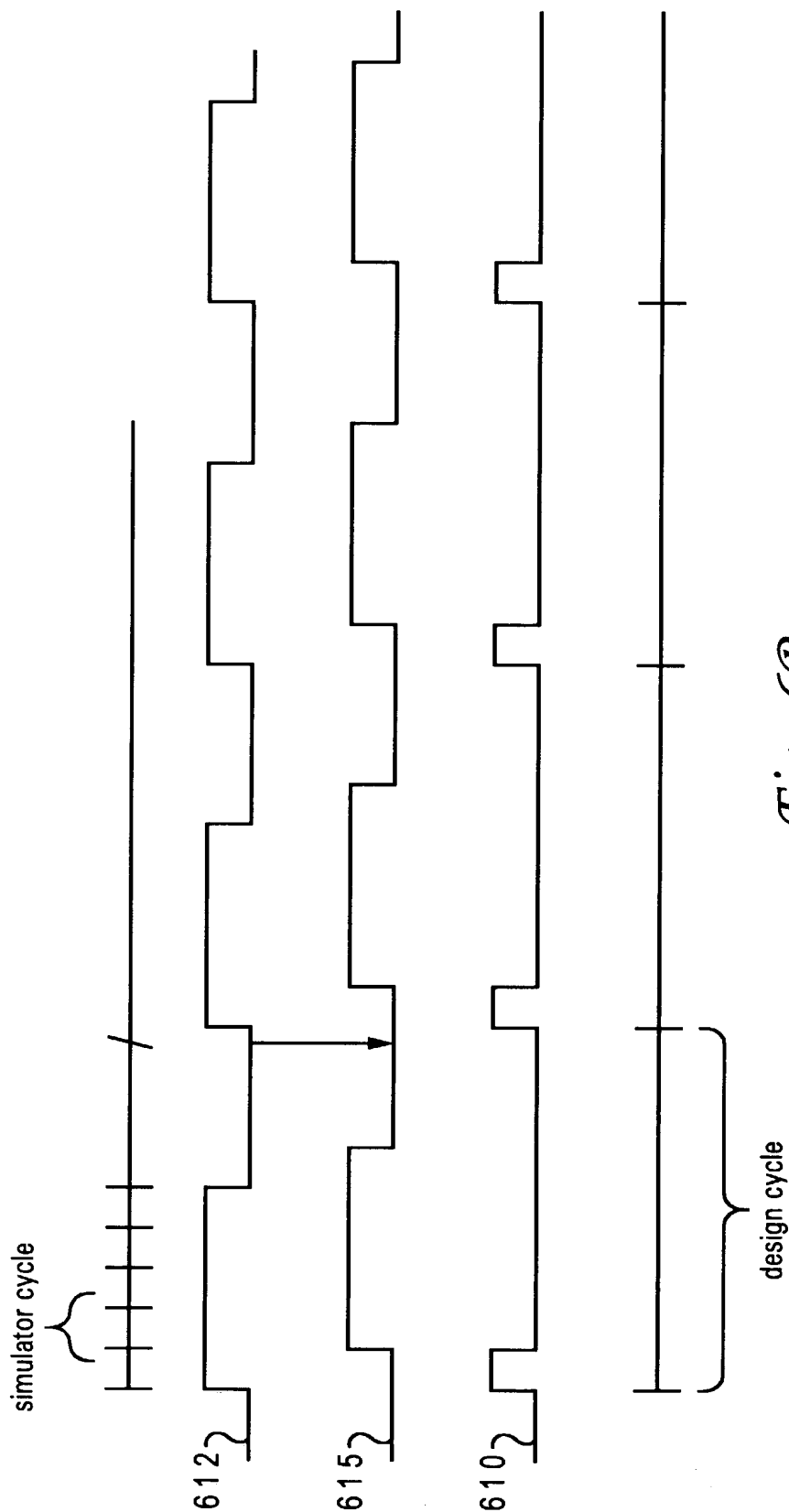


Fig. 6B

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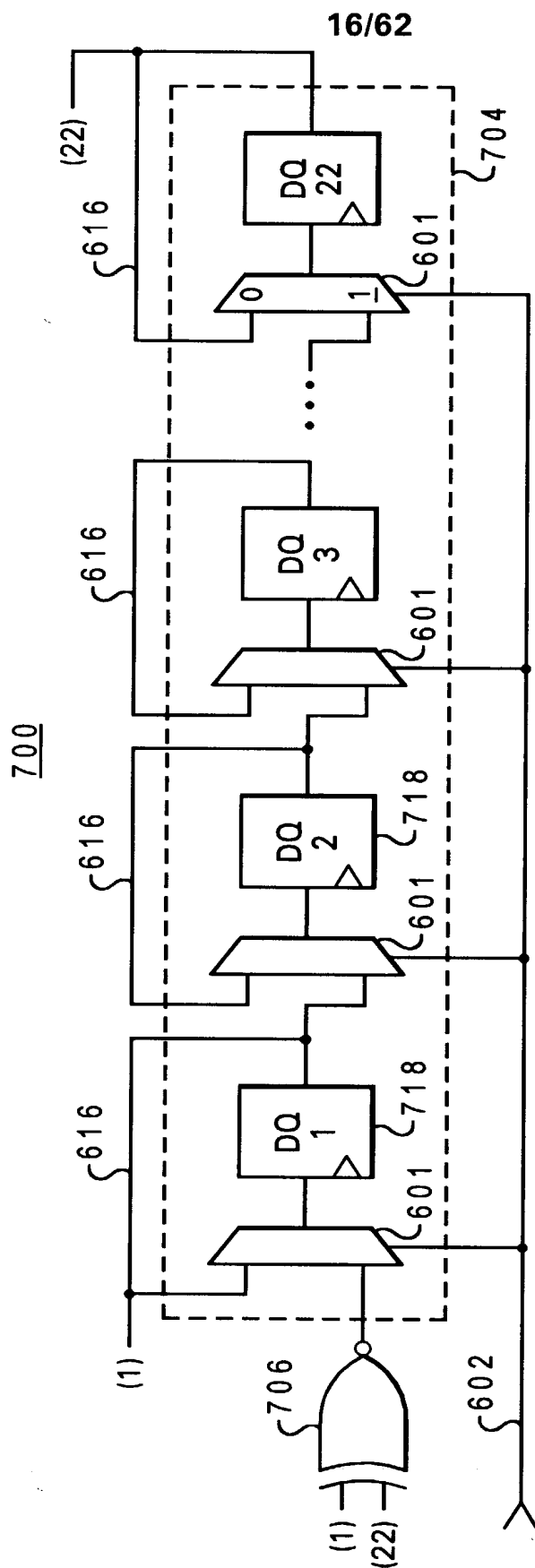


Fig. 7

800

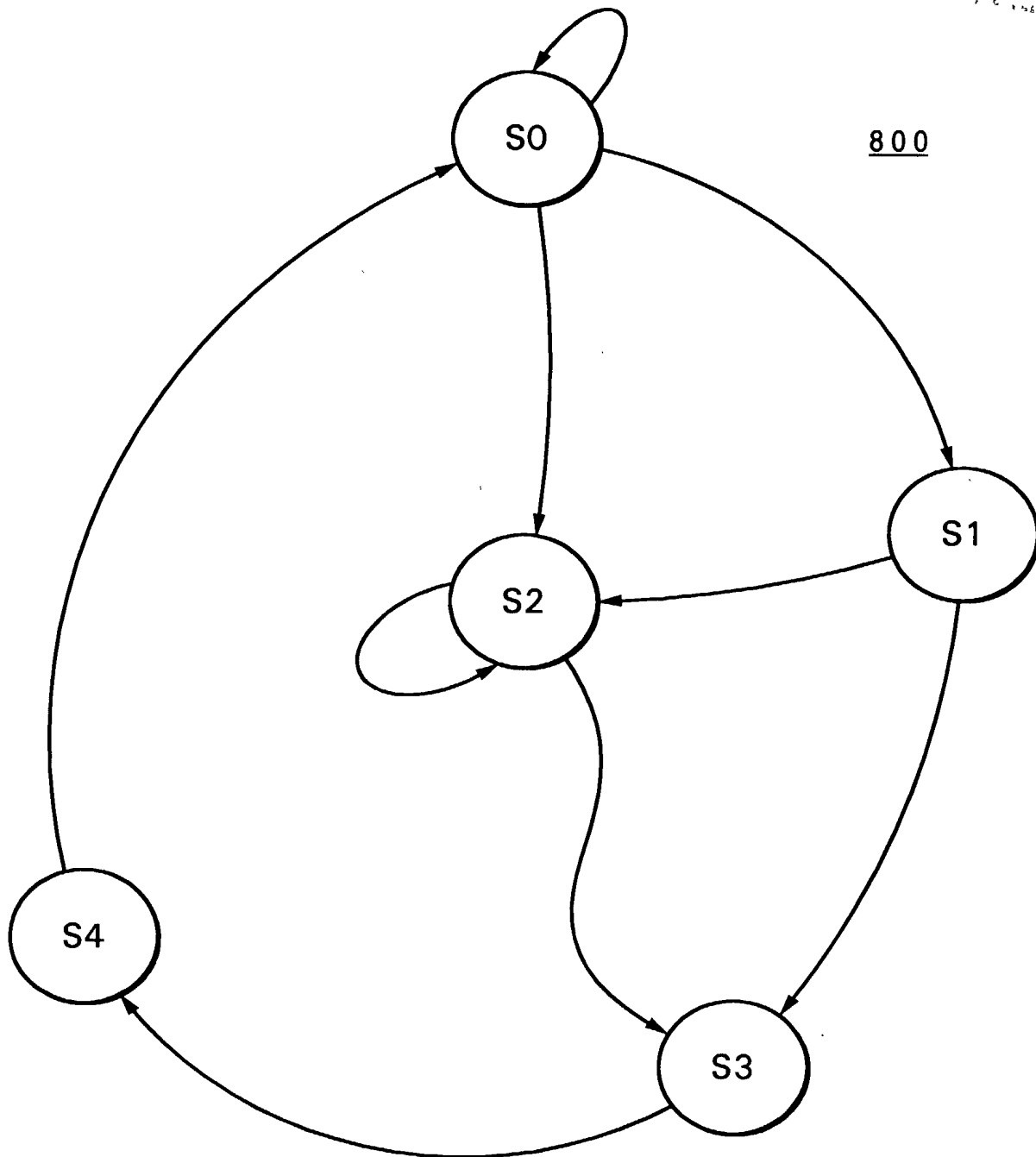


Fig. 8A

Prior Art

entity FSM : FSM

850

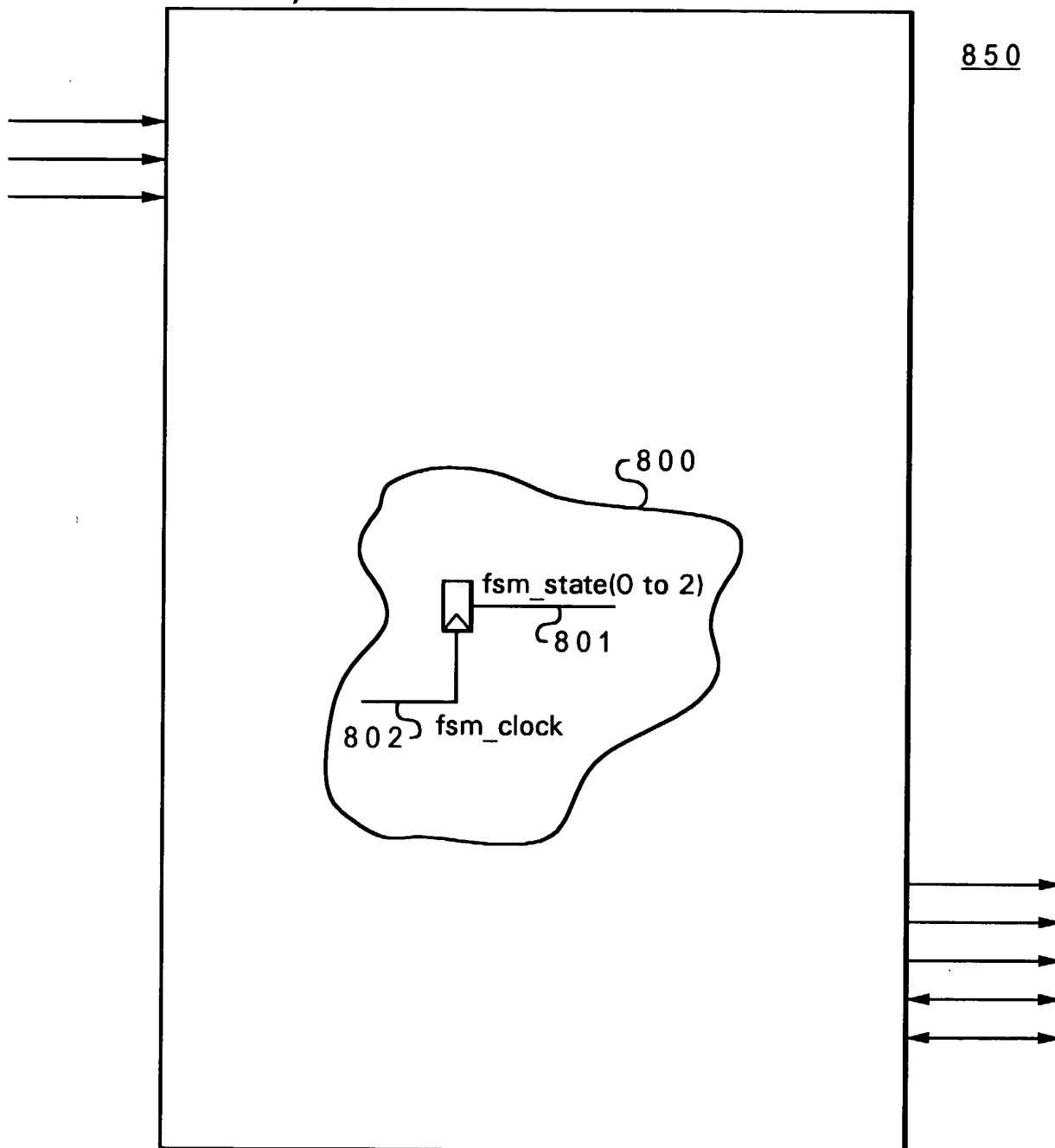


Fig. 8B

Prior Art

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ENTITY FSM IS

PORT(
 ports for entity fsm....
);

ARCHITECTURE FSM OF FSM IS

BEGIN

 ... HDL code for FSM and rest of the entity ...

 fsm_state(0 to 2) <= ... Signal 801 ...

853	{	--!! Embedded FSM : examplefsm;	}	852	}	860
859	{	--!! clock : (fsm_clock);				
854	{	--!! state_vector : (fsm_state(0 to 2));				
855	{	--!! states : (S0, S1, S2, S3, S4);				
856	{	--!! state_encoding : ('000', '001', '010', '011', '100');				
857	{	--!! arcs : (S0 => S0, S0 => S1, S0 => S2, (S1 => S2, S1 => S3, S2 => S2, (S2 => S3, S3 => S4, S4 => S0);				
858	{	--!! End FSM;				

END;

Fig. 8C

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entity FSM : FSM

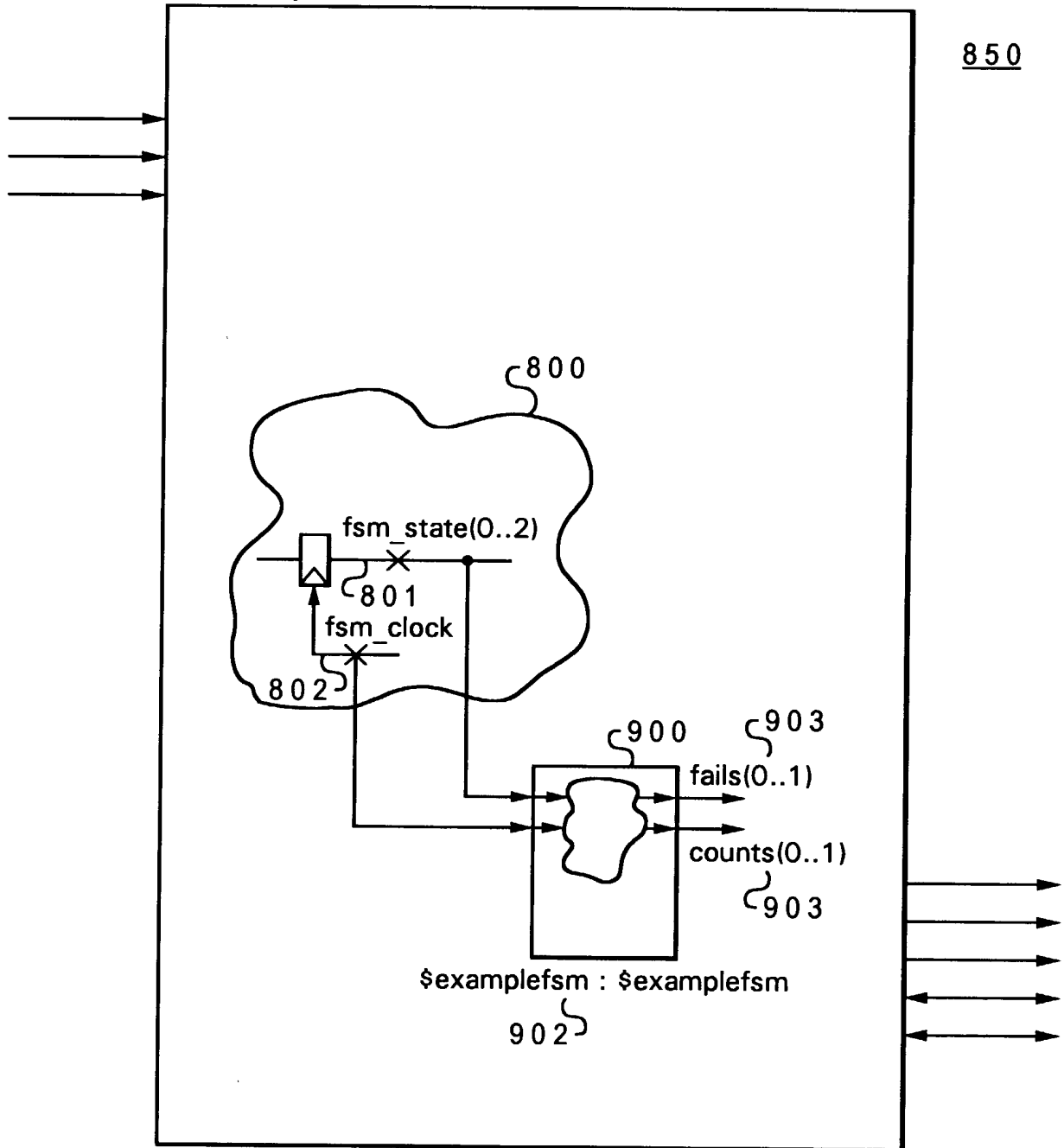
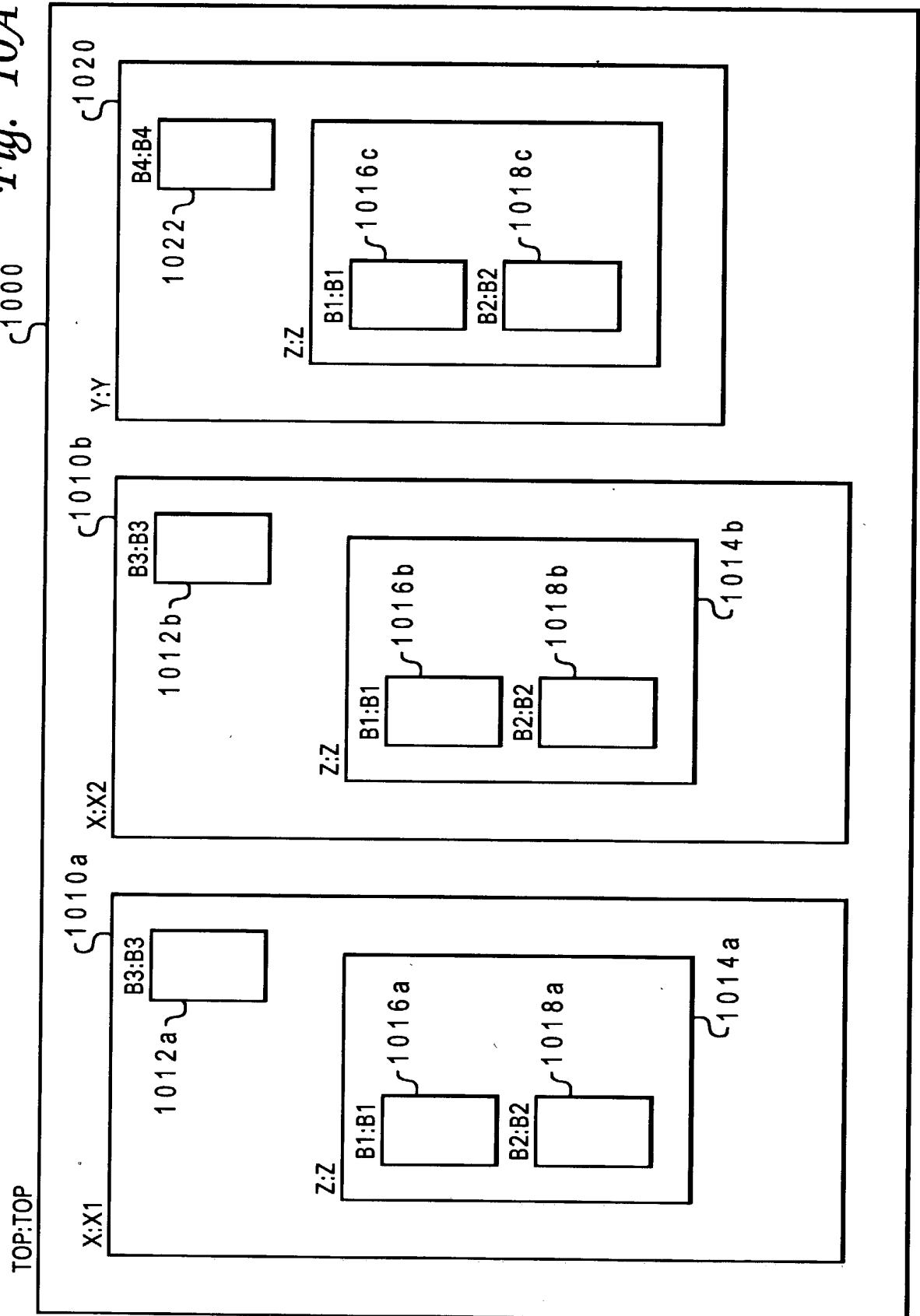


Fig. 9

Fig. 10A



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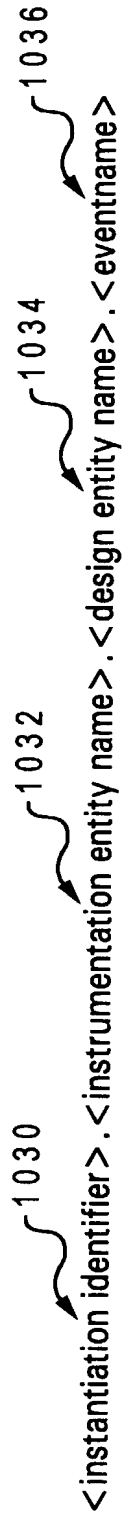


Fig. 10B

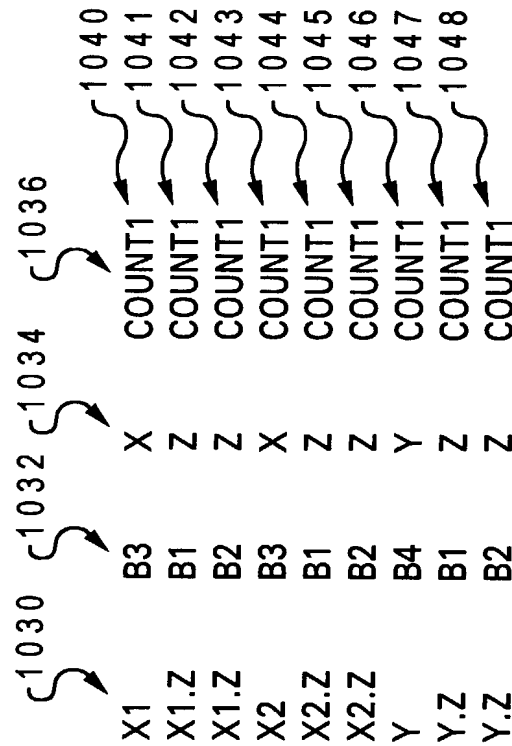


Fig. 10C

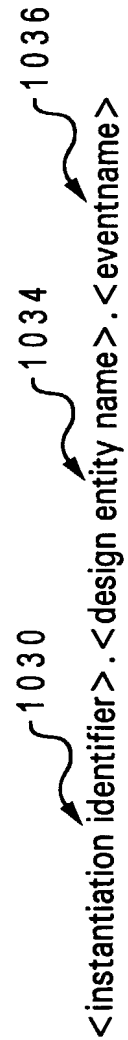
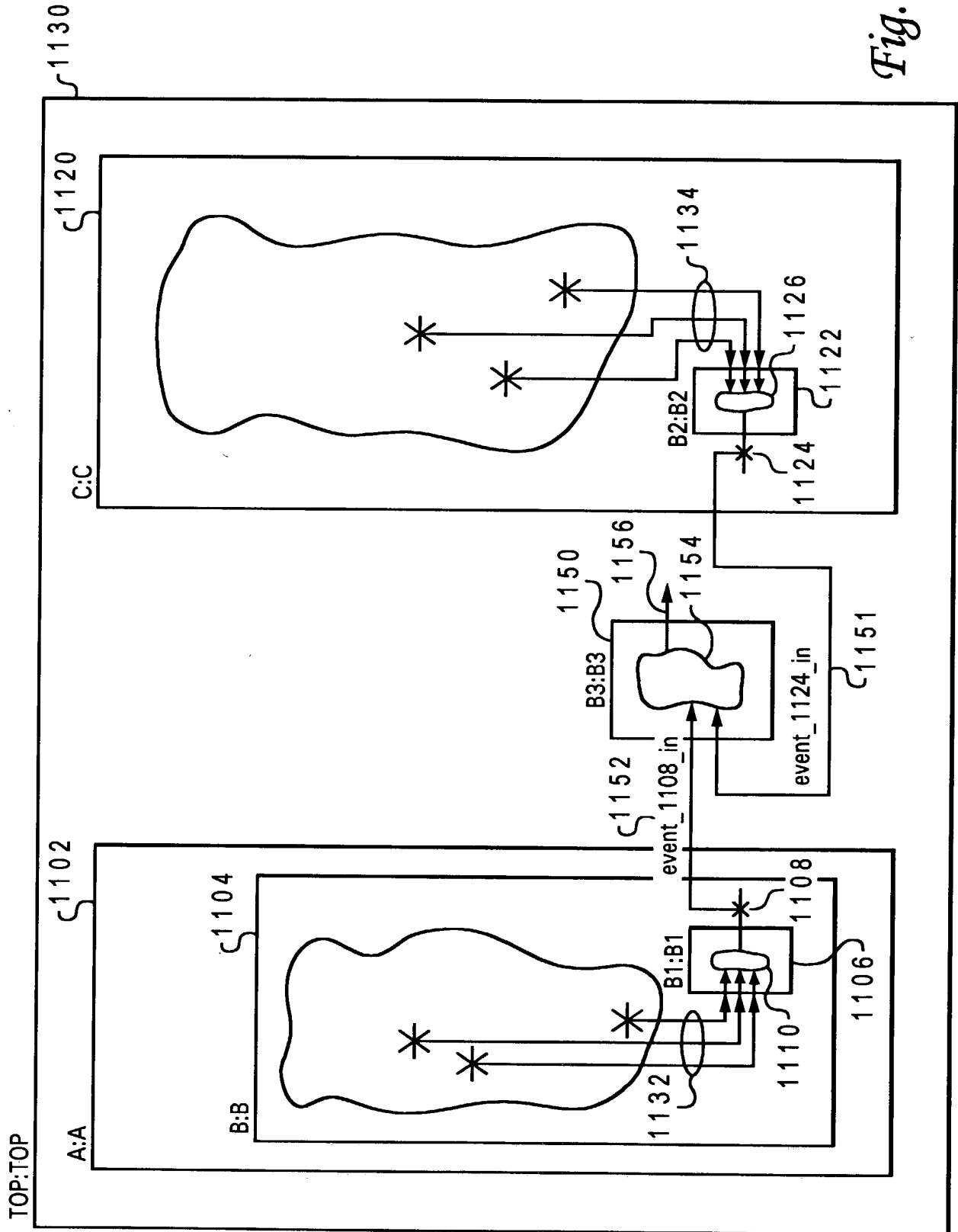


Fig. 10D



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--!! Inputs
--!! event_1108_in <= C.[B2.count.event_1108];
--!! event_1124_in <= A.B.[B1.count.event_1124];
--!! End Inputs

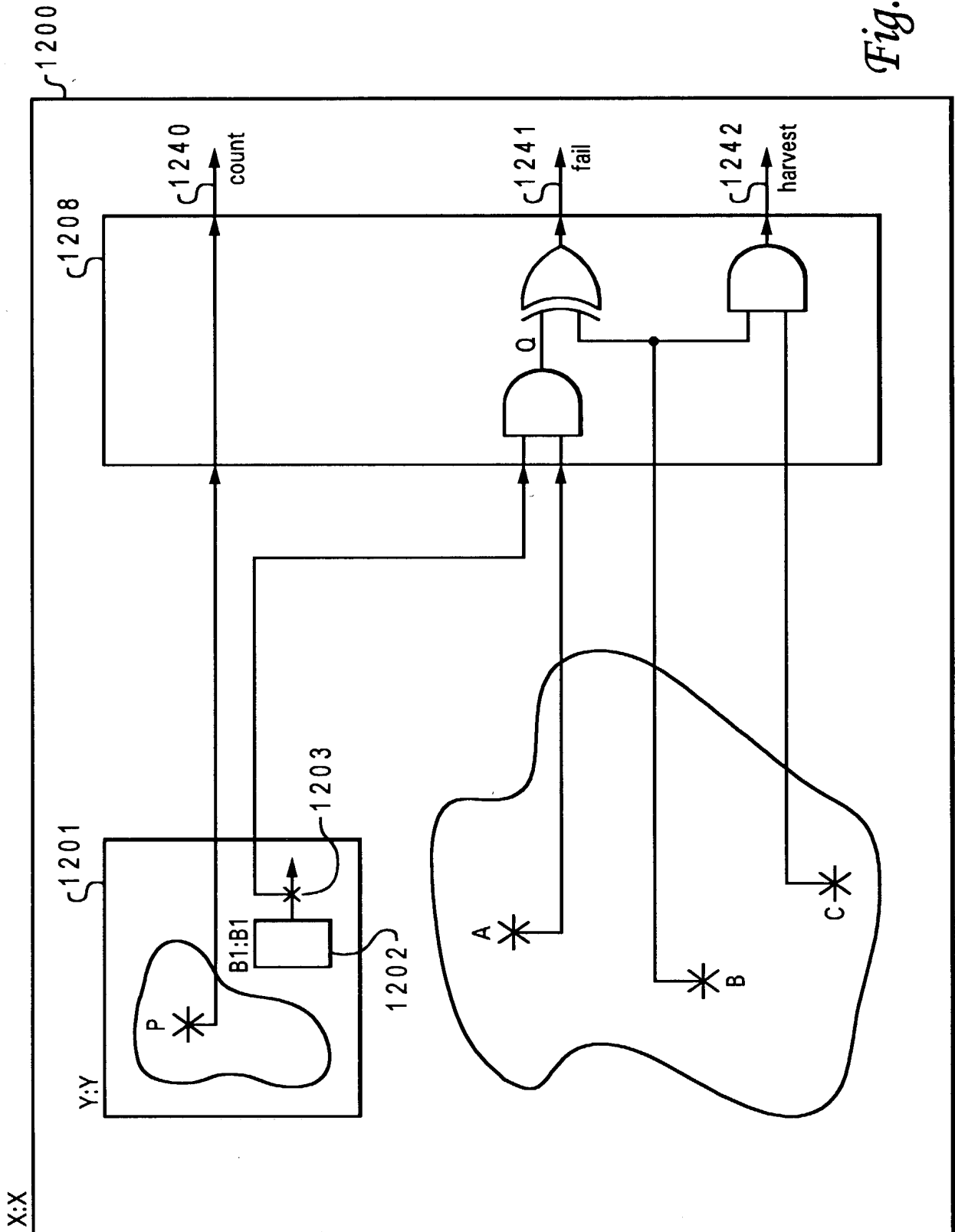
1163 1165 1161 1162 1164 1166

Fig. 11B

--!! Inputs
--!! event_1108_in <= C.[count.event_1108];
--!! event_1124_in <= B.[count.event_1124];
--!! End Inputs

1171 1172

Fig. 11C



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```

ENTITY X IS
    PORT(
        :
        :
        :
    );

    ARCHITECTURE example of X IS
    BEGIN
        .
        .
        .
        ... HDL code for X ...
        .
        .
        .
    END;
1 2 2 1 { Y:Y
        PORT MAP(
            :
            :
            );
1 2 2 2 { A <= ....
        B <= ....
        C <= ....
1 2 2 3 { --!! [count, countname0, clock] <= Y.P;
        --!! Q <= Y. [B1.count.count1] AND A;
        --!! [fail, failname0, "fail,msg"] <= Q XOR B;
        --!! [harvest, harvestname0, "harvest msg"] <= B AND C;
        END;
1 2 3 0
1 2 3 2
1 2 3 4
1 2 3 6
1 2 2 0
    
```

Fig. 12B

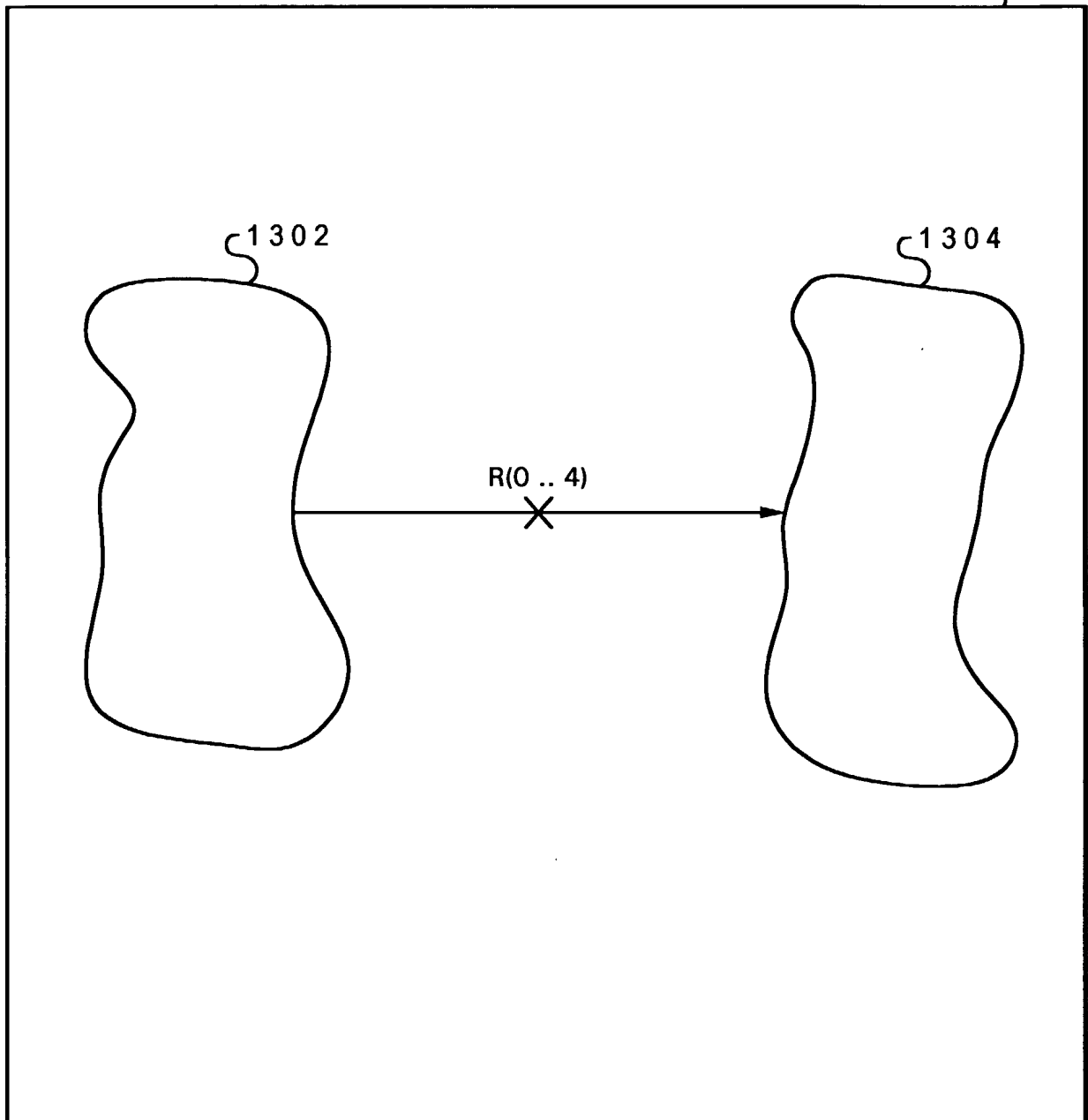


Fig. 13A

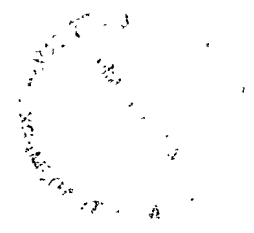
Fig. 13B

SECRET

Fig. 13C

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ENTITY FOO IS

PORT(:
 :
 :
);

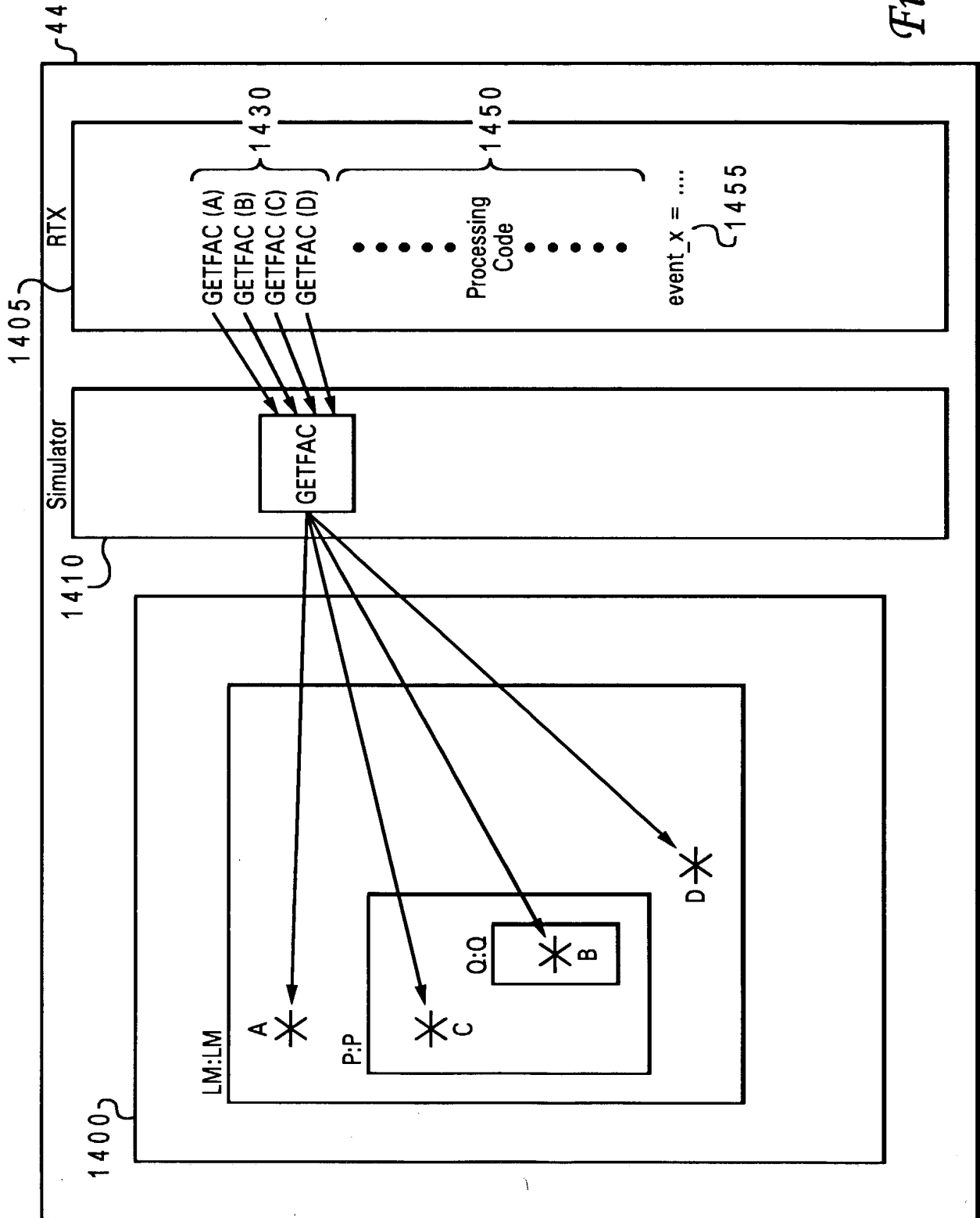
ARCHITECTURE example of FOO IS

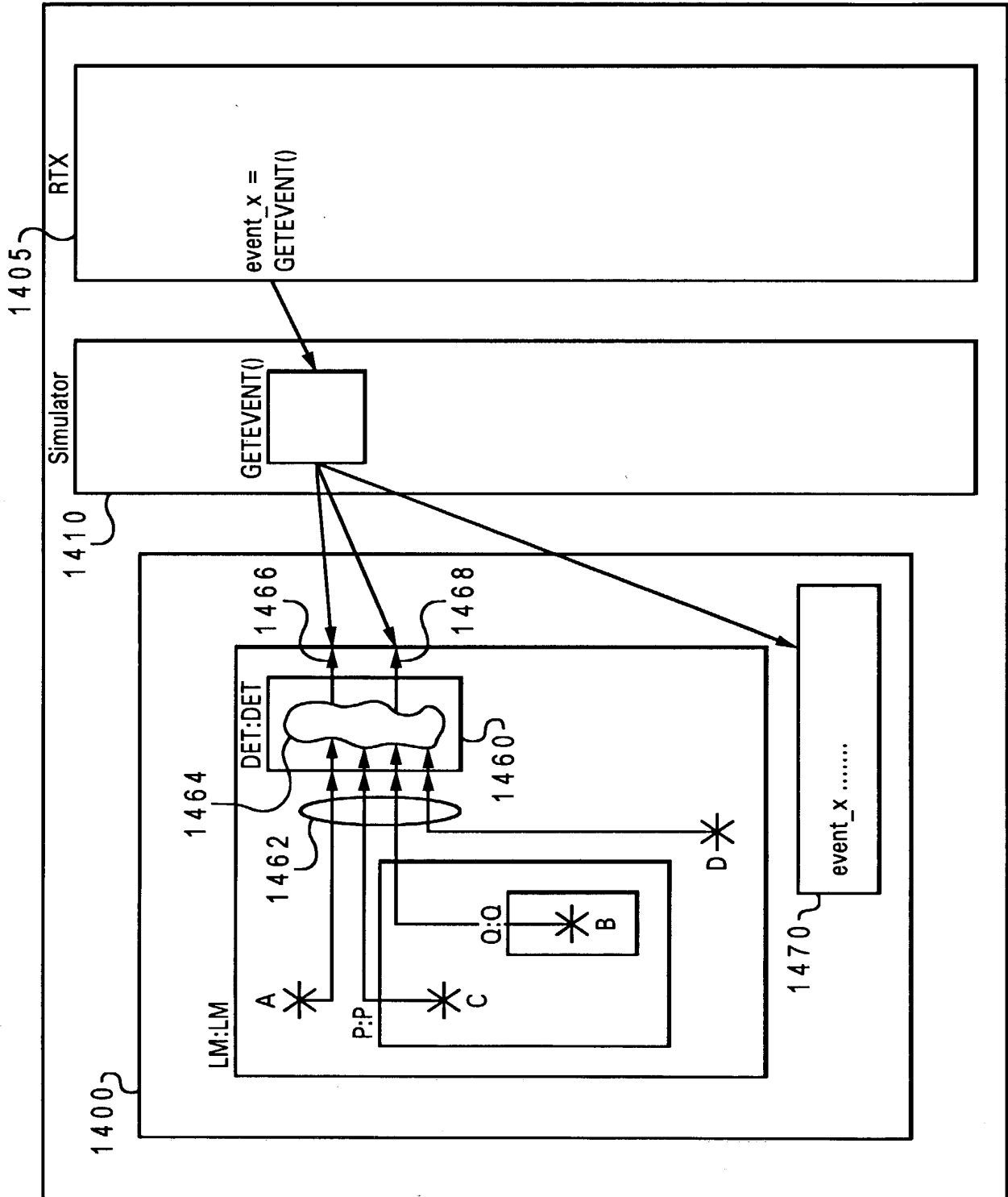
BEGIN

.
 .
 .
 .
 .
 R <=
 .
 .
 .
 .

1380 { --!! R_IN <= {R}; 1381
 --!! 1382
 --!!
 --!! R_OV(0 to 4) <=; 1383
 --!! RT <=;
 --!! [override, R_OVRRIDE, R(0 .. 4), RT] <= R_OV(0 to 4); 1384

Fig. 13D






```

PORT(      A      :      IN std_ulogic;
           B      :      IN std_ulogic_vector(0 to 5);
           C      :      IN std_ulogic;
           D      :      IN std_ulogic;
           :
           :
           :
           event_x :      OUT std_ulogic_vector(0 to 2);
           x_here  :      OUT std_ulogic;
);

```

```

--!! BEGIN
--!! Design Entity: LM;

--!! Inputs
--!! A  =>  A;
--!! B  =>  P.Q.B;
--!! C  =>  P.C;
--!! D  =>  D;
--!! End Inputs

--!! Detections
--!! <event_x>:event_x(0 to 2) [x_here];
--!! End Detections

--!! End;

ARCHITECTURE example of DET IS

BEGIN

    ... HDL code ...

END;

```

Fig. 14C

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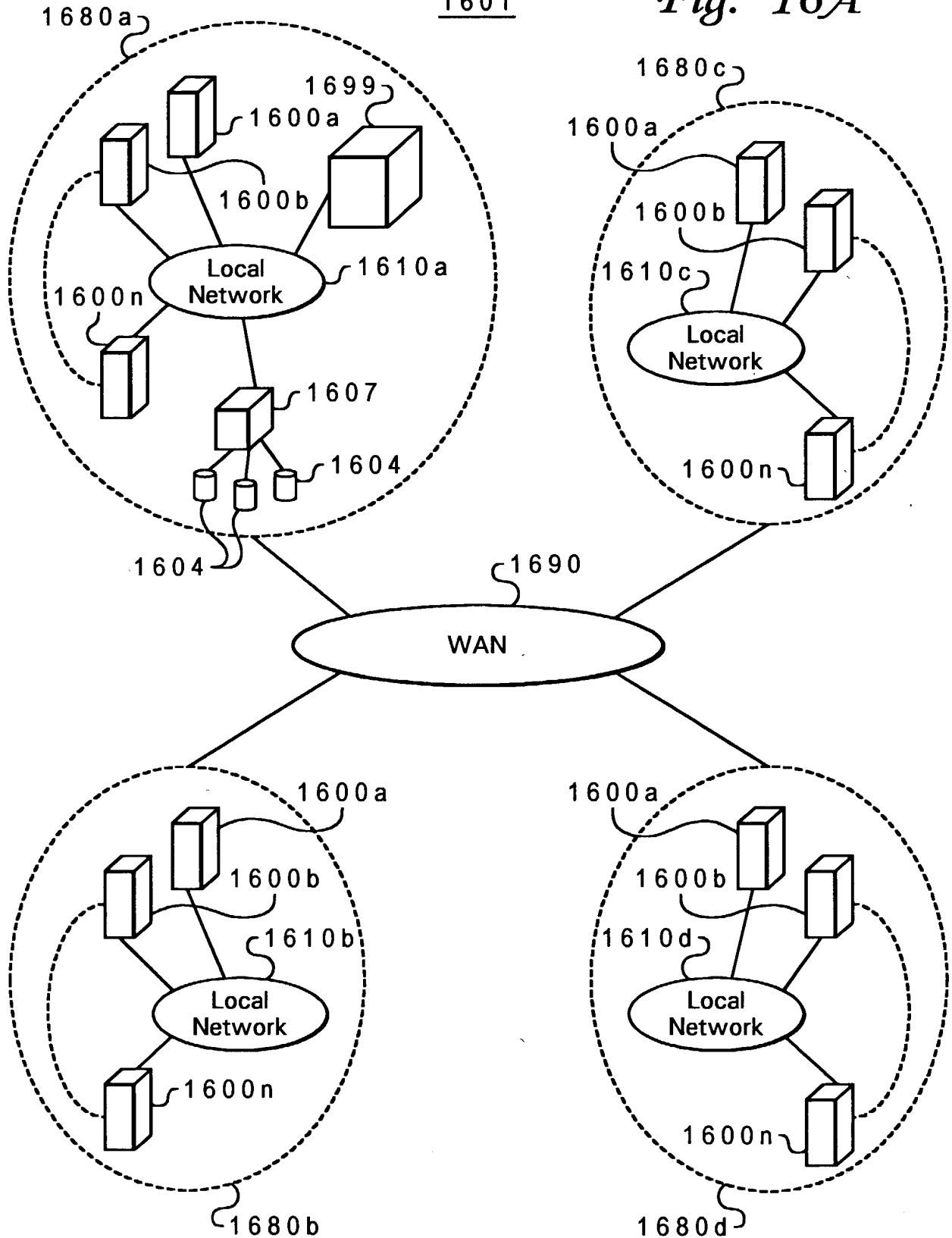
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1660

	1 6 6 1	1 6 6 2			
1 6 6 3	1:	X1	B3	X	COUNT1
	2:	X1.Z	B1	Z	COUNT1
	3:	X1.Z	B2	Z	COUNT1
	4:	X2	B3	X	COUNT1
	5:	X2.Z	B1	Z	COUNT1
	6:	X2.Z	B2	Z	COUNT1
	7:	Y	B4	Y	COUNT1
	8:	Y.Z	B1	Z	COUNT1
	9:	Y.Z	B2	Z	COUNT1

Fig. 15

Fig. 16A



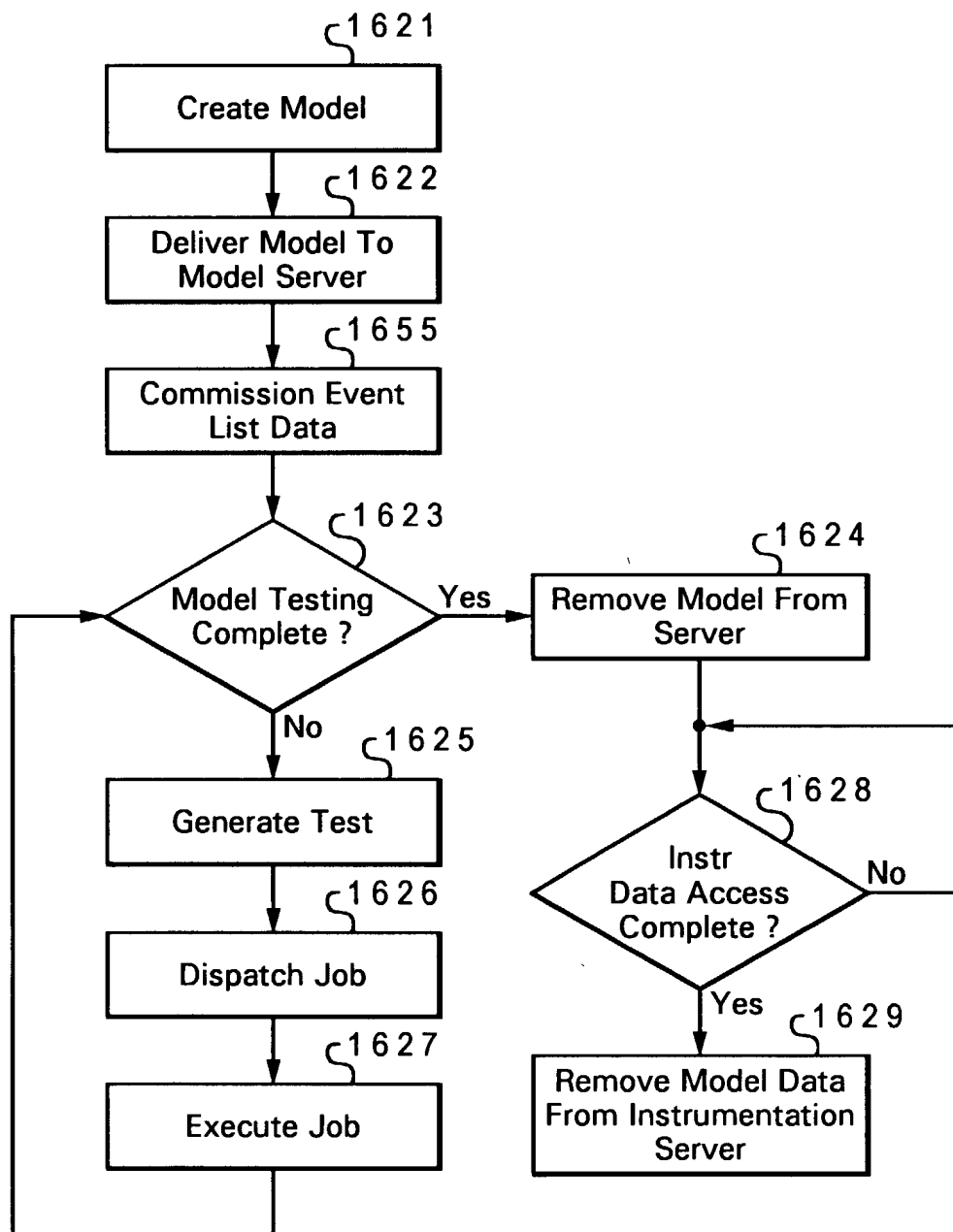


Fig. 16B

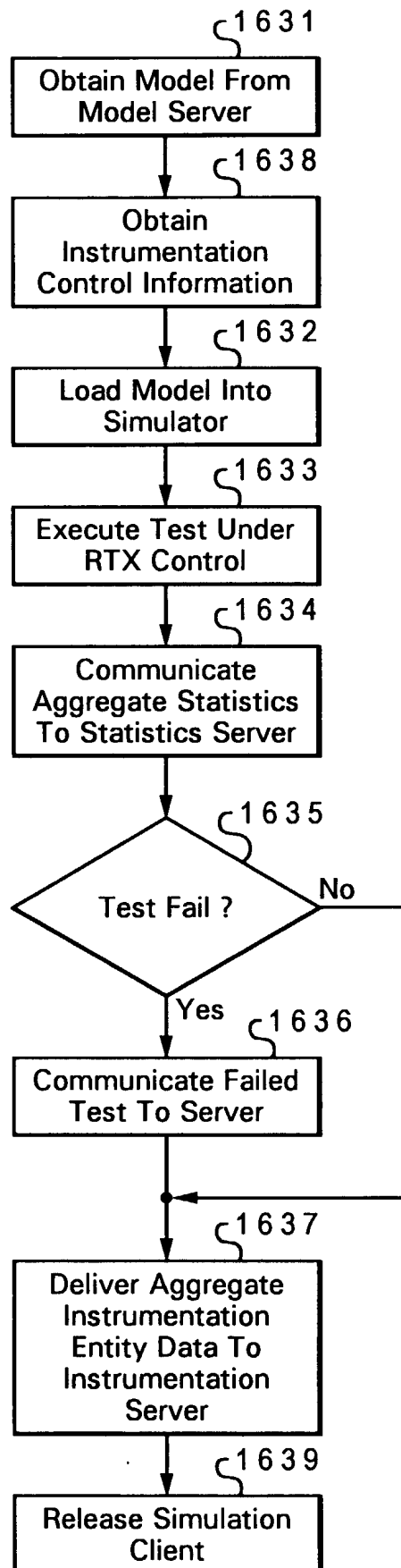


Fig. 16C

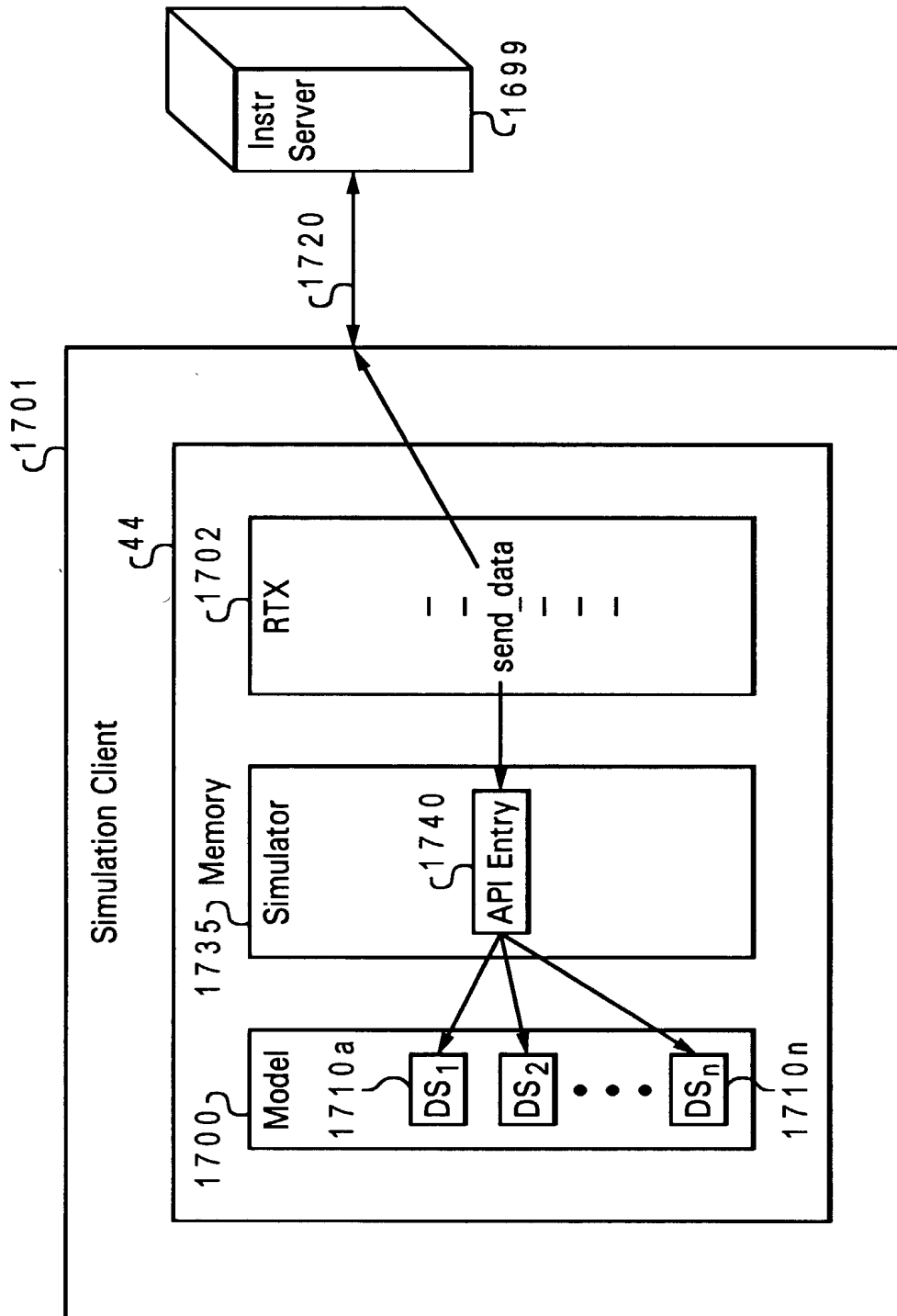


Fig. 17A



1750

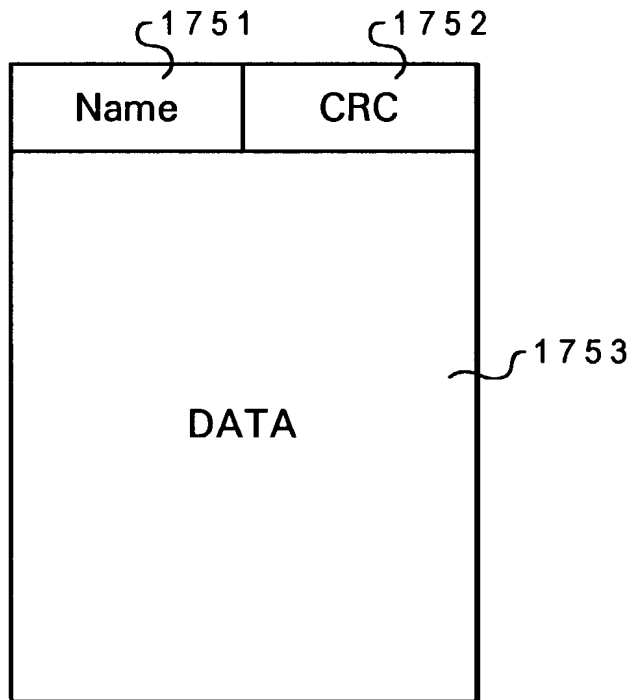


Fig. 17B

Fig. 17C

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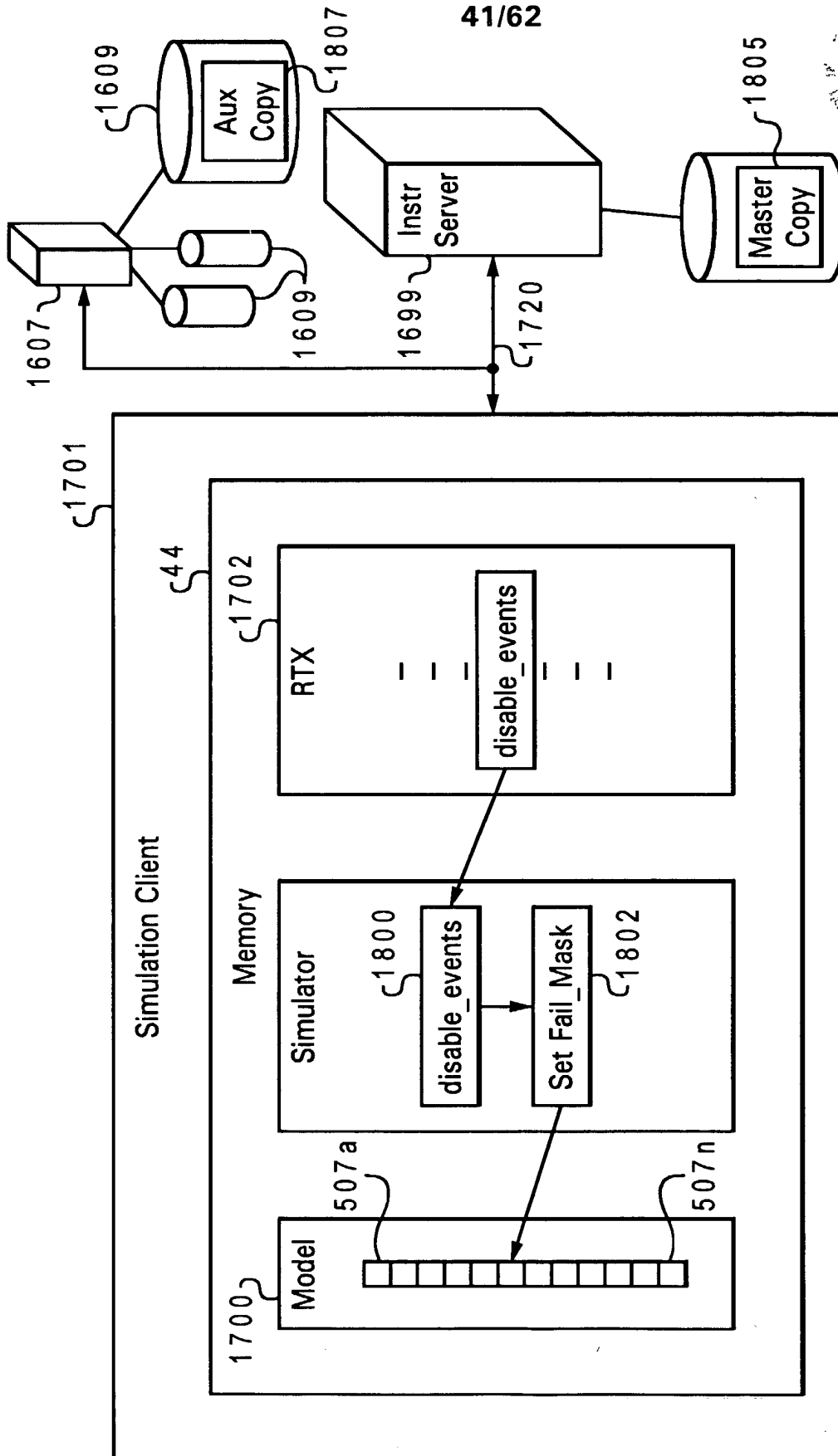
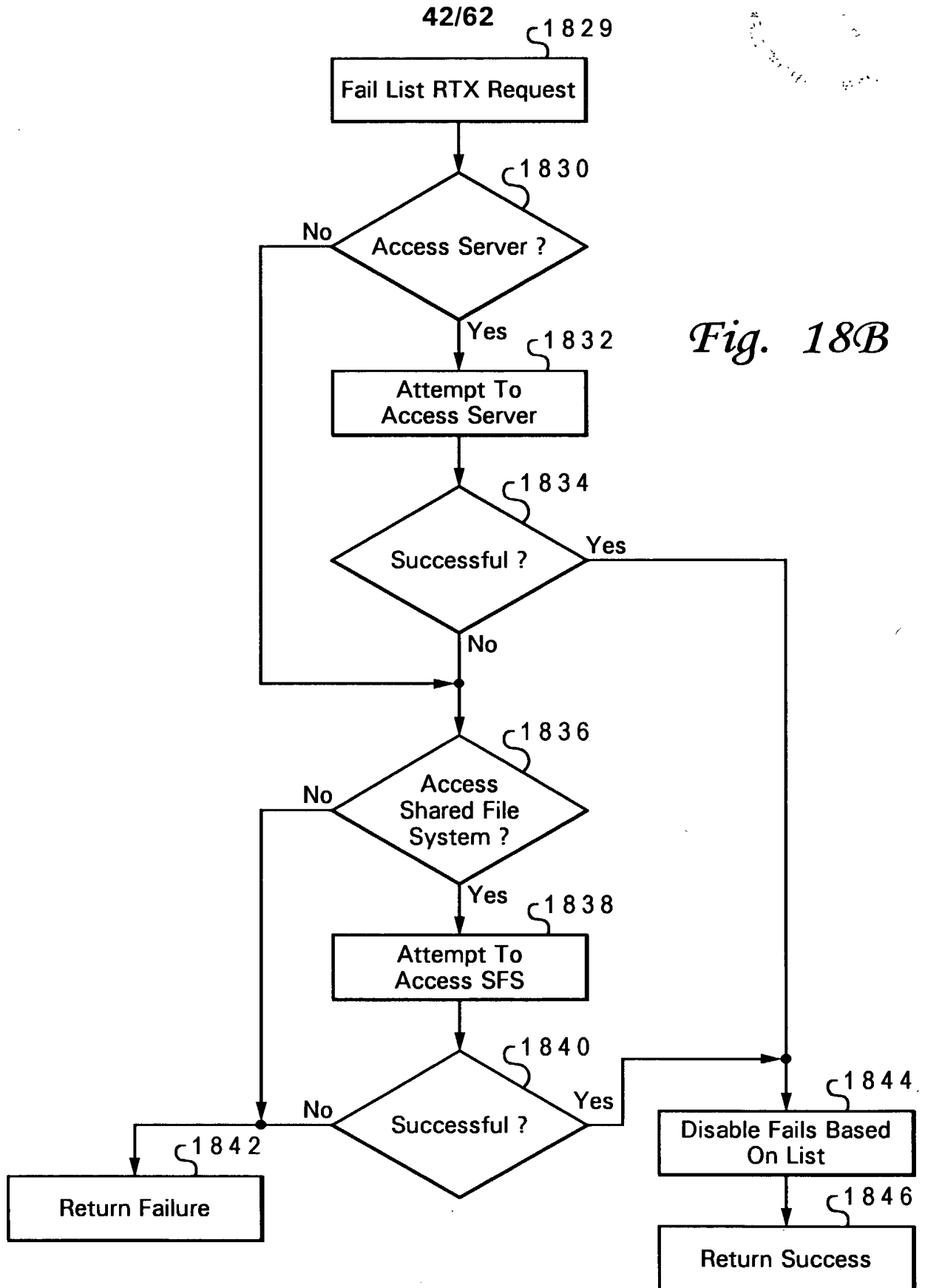


Fig. 18A

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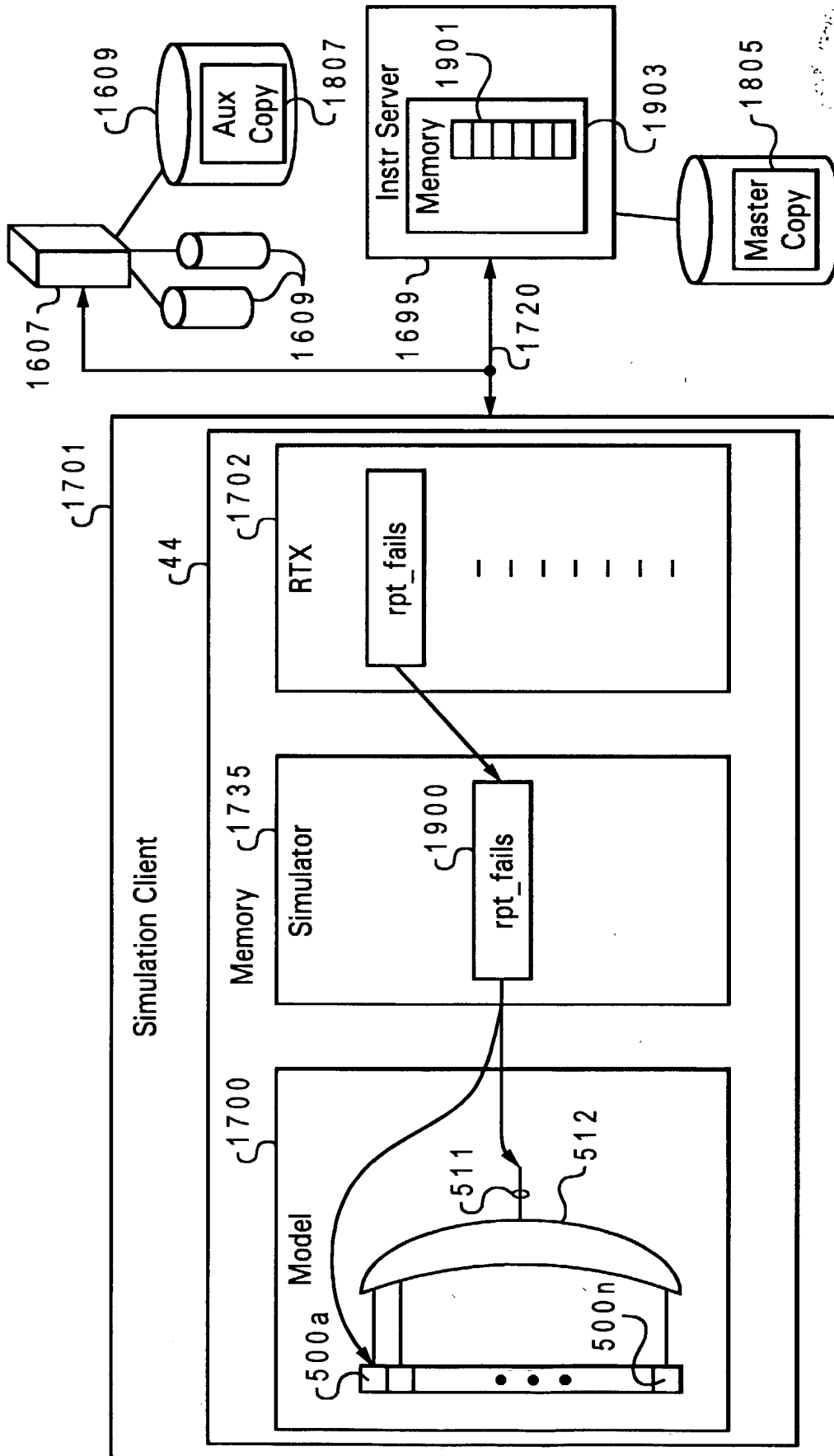
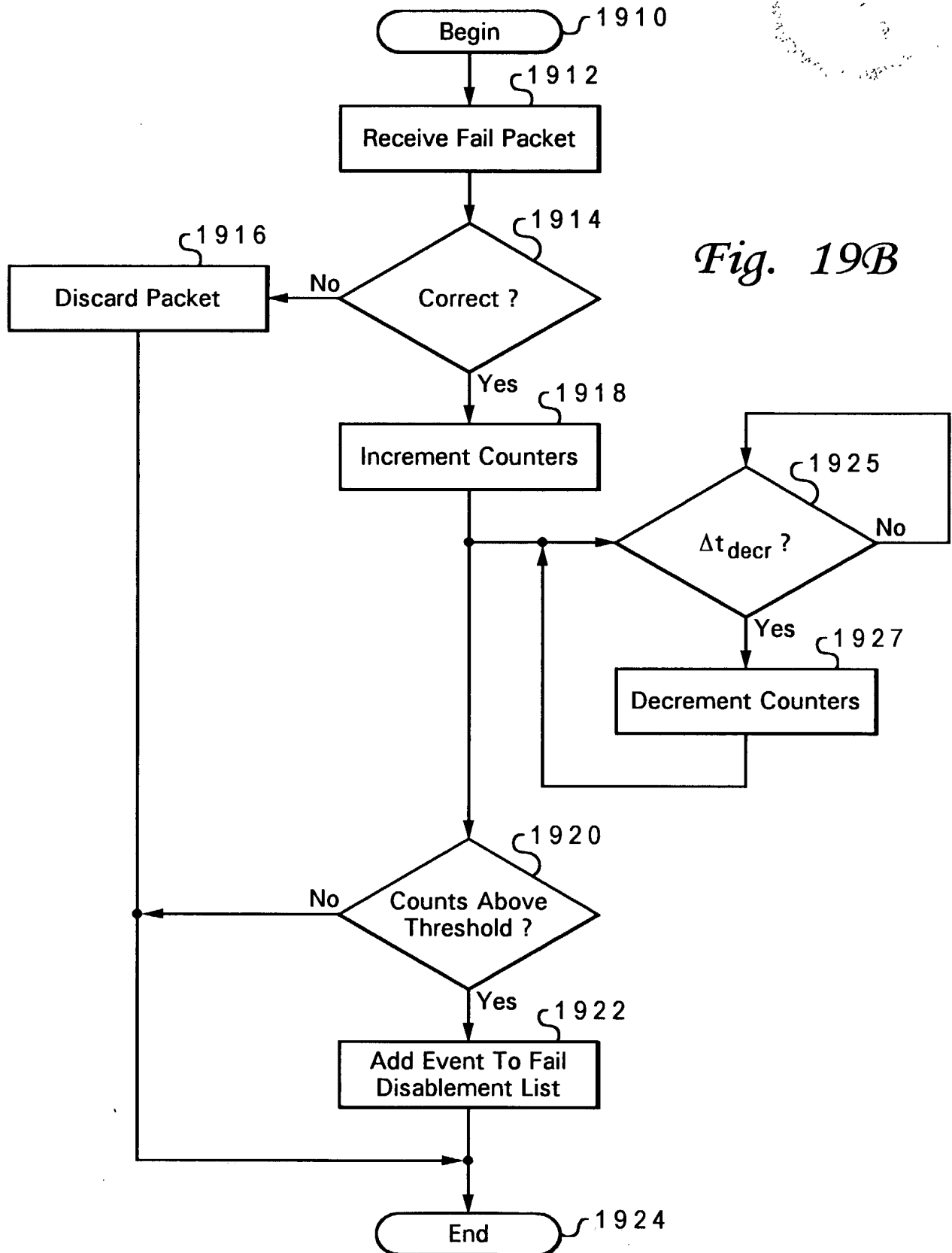


Fig. 19A

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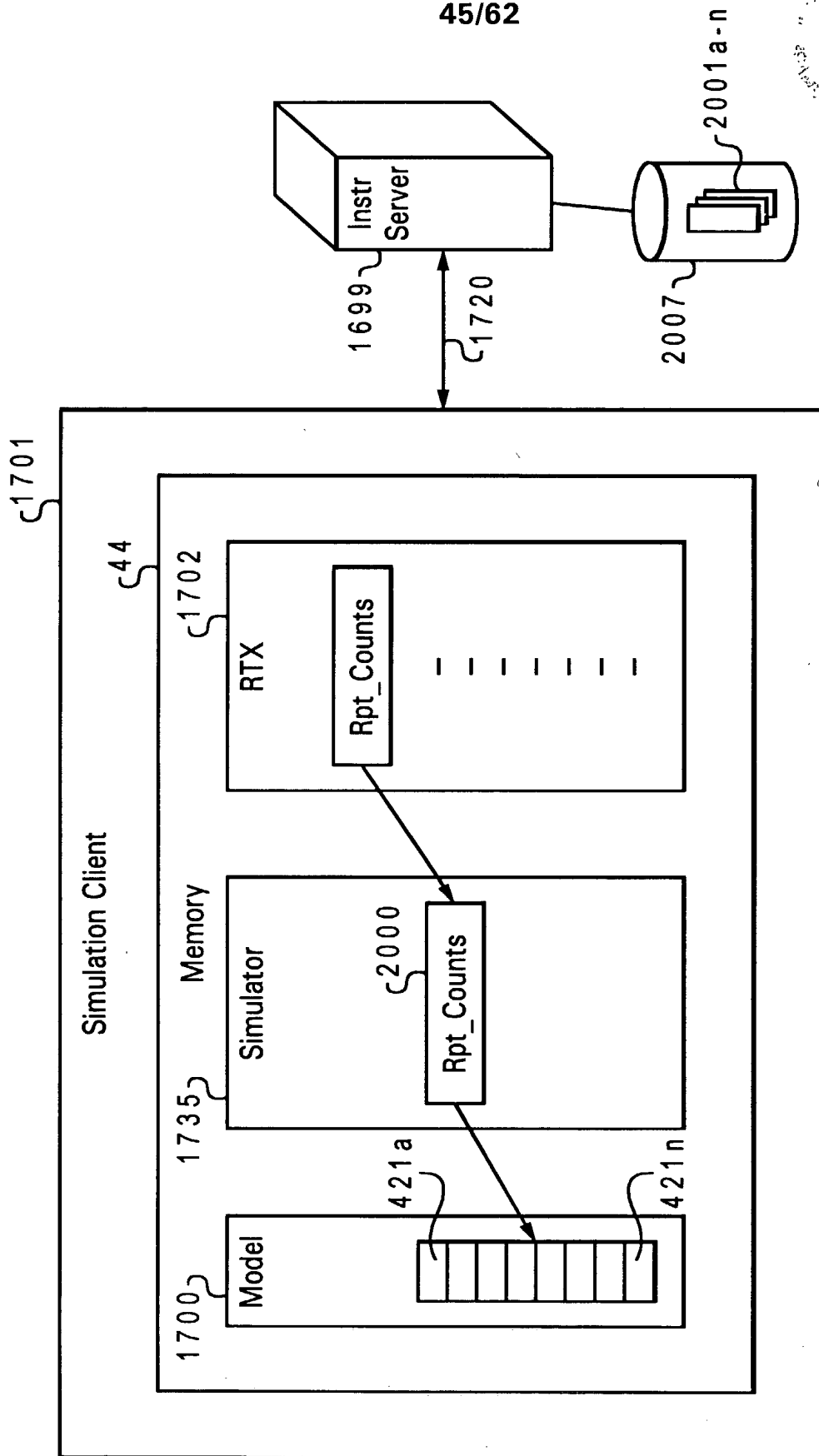


Fig. 20A

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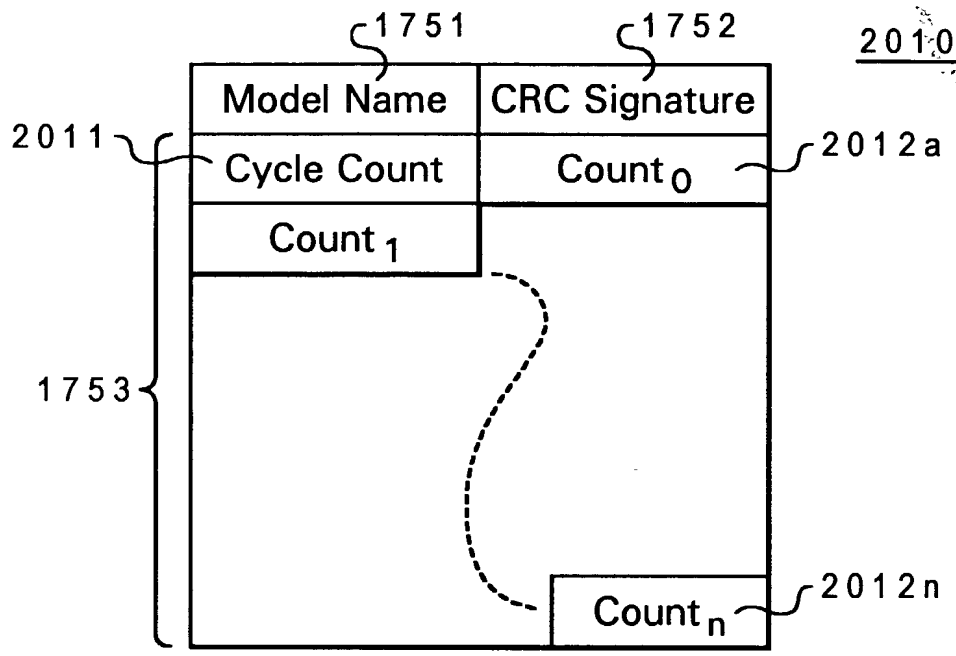


Fig. 20B

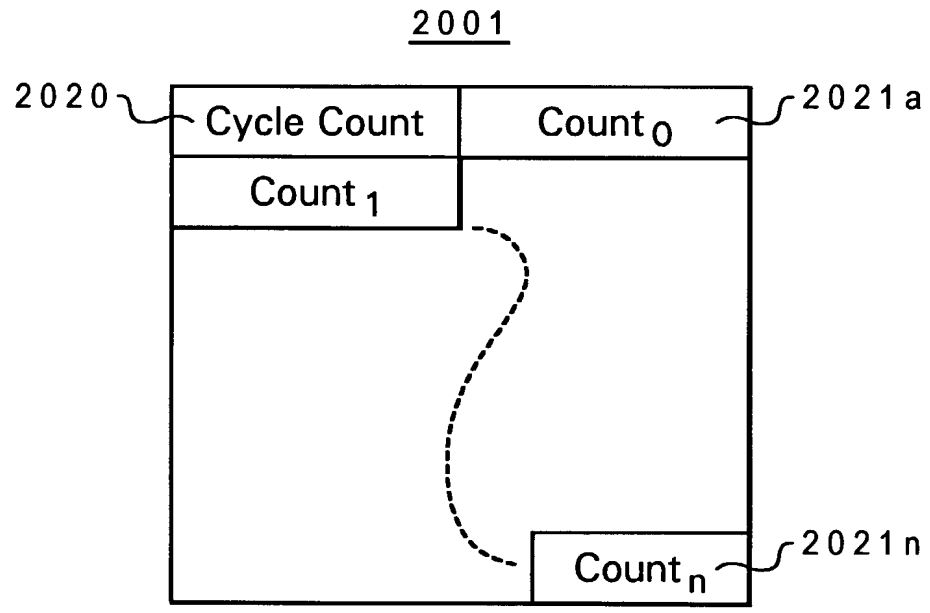


Fig. 20C

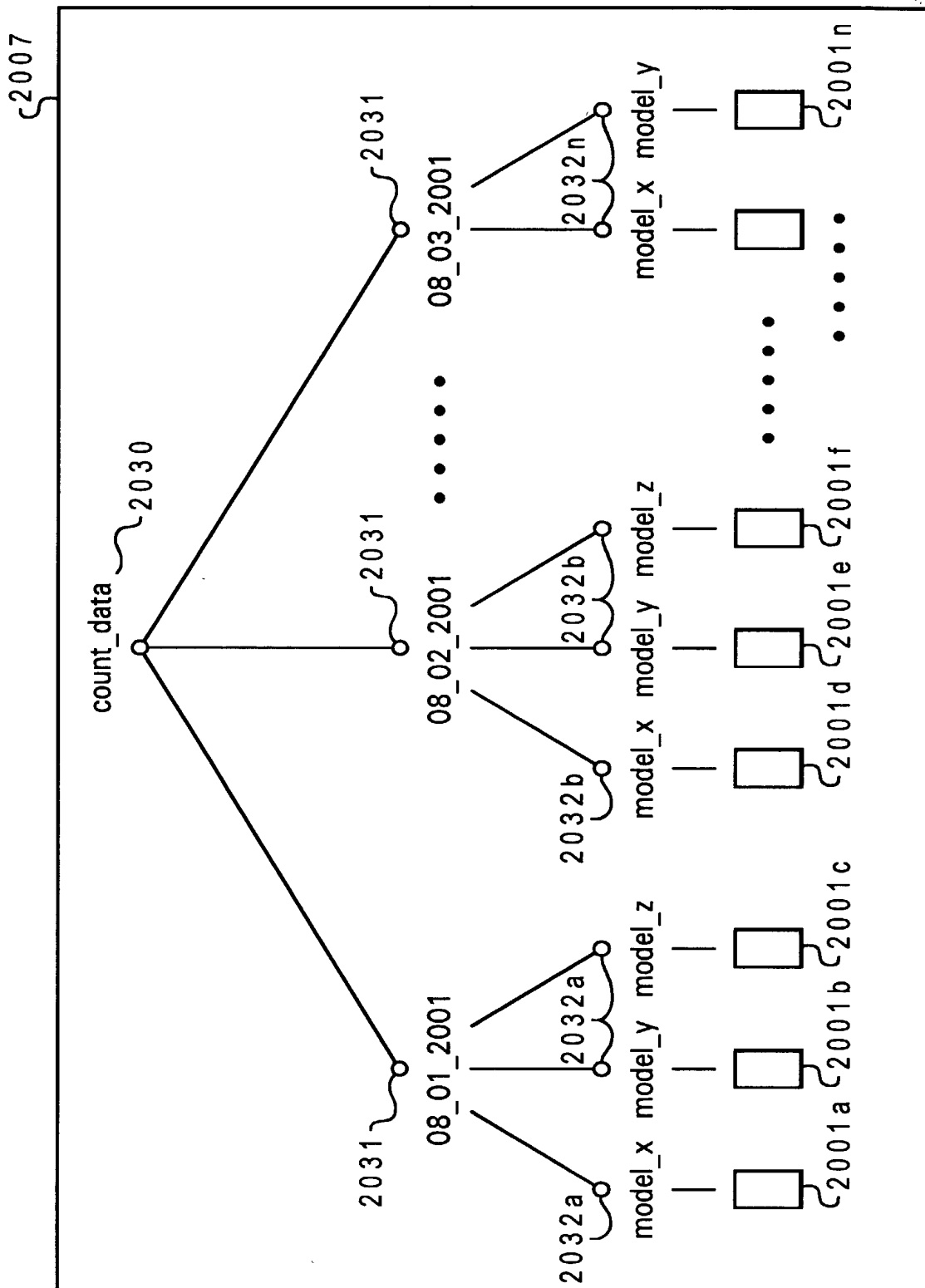


Fig. 20D

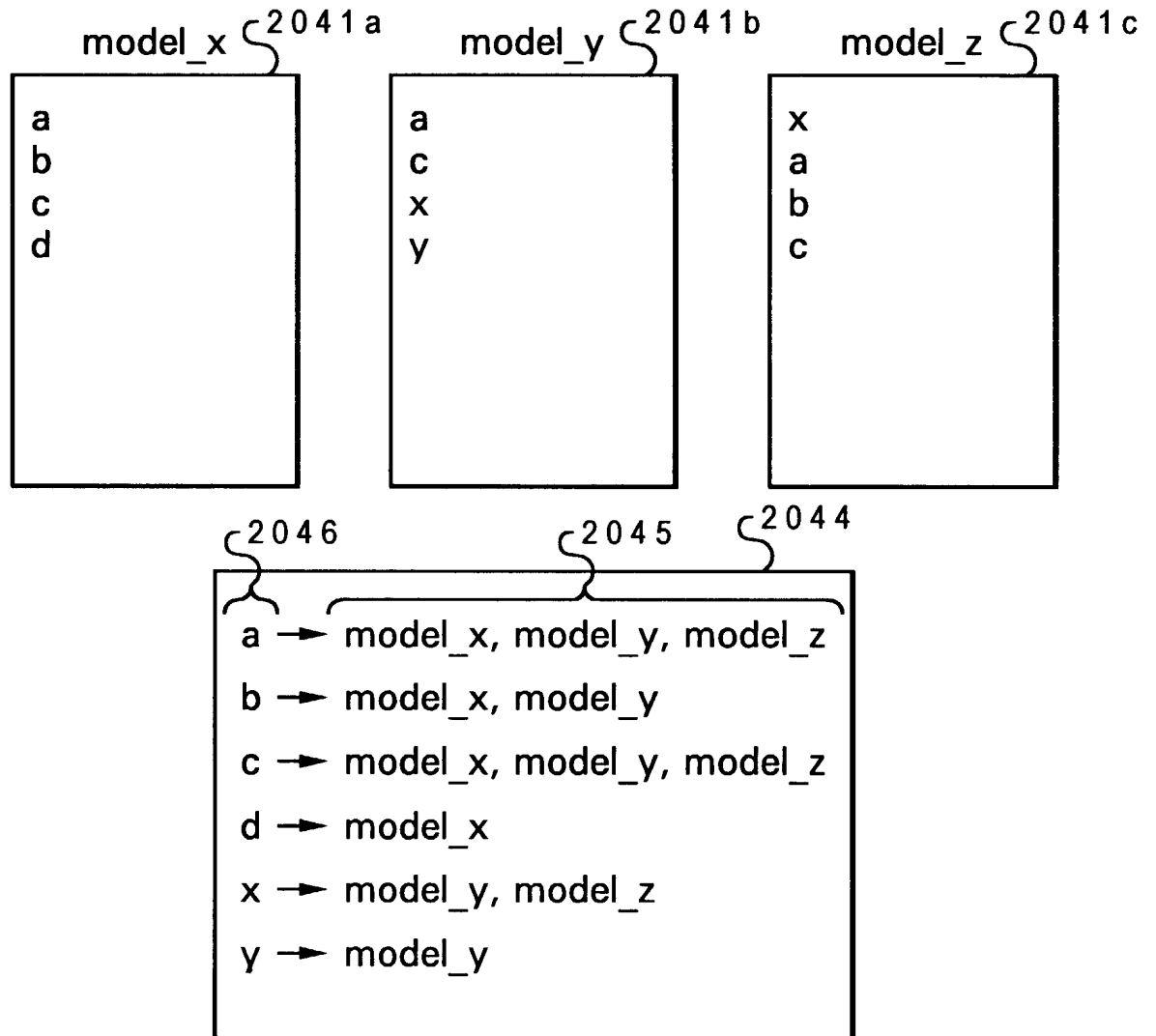


Fig. 20E

00007262 14:5003

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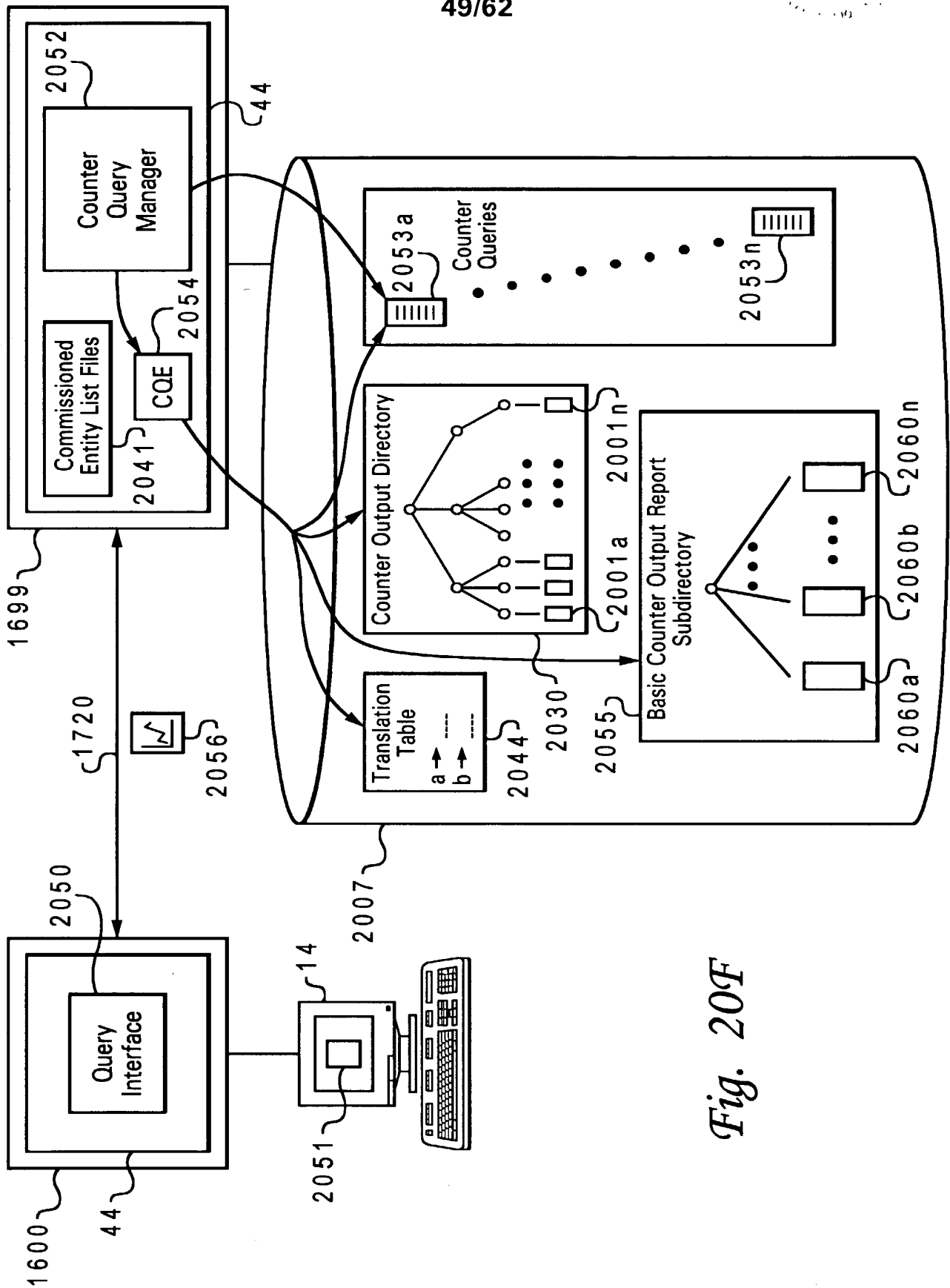
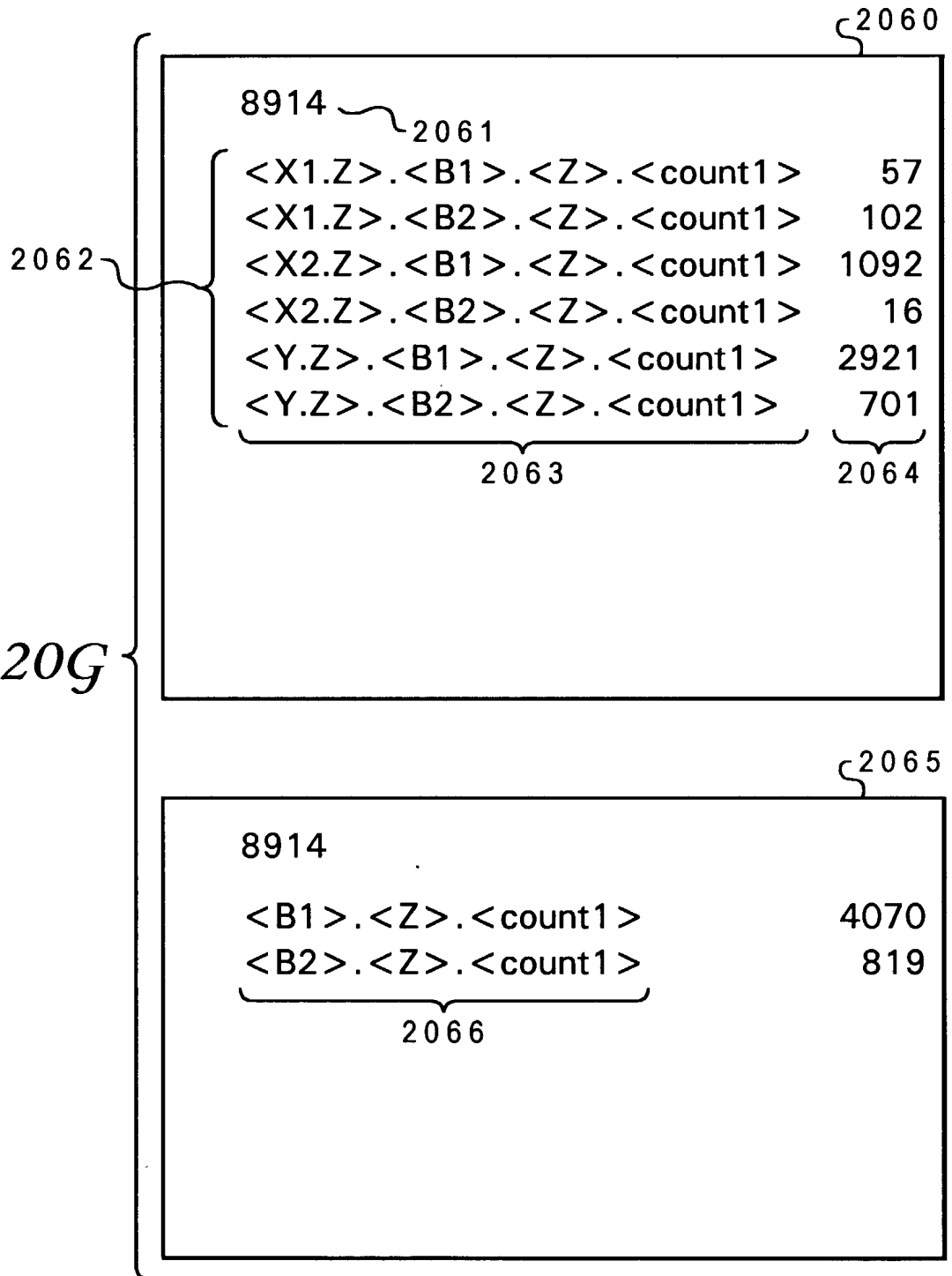
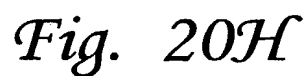


Fig. 20F



Fig. 20G





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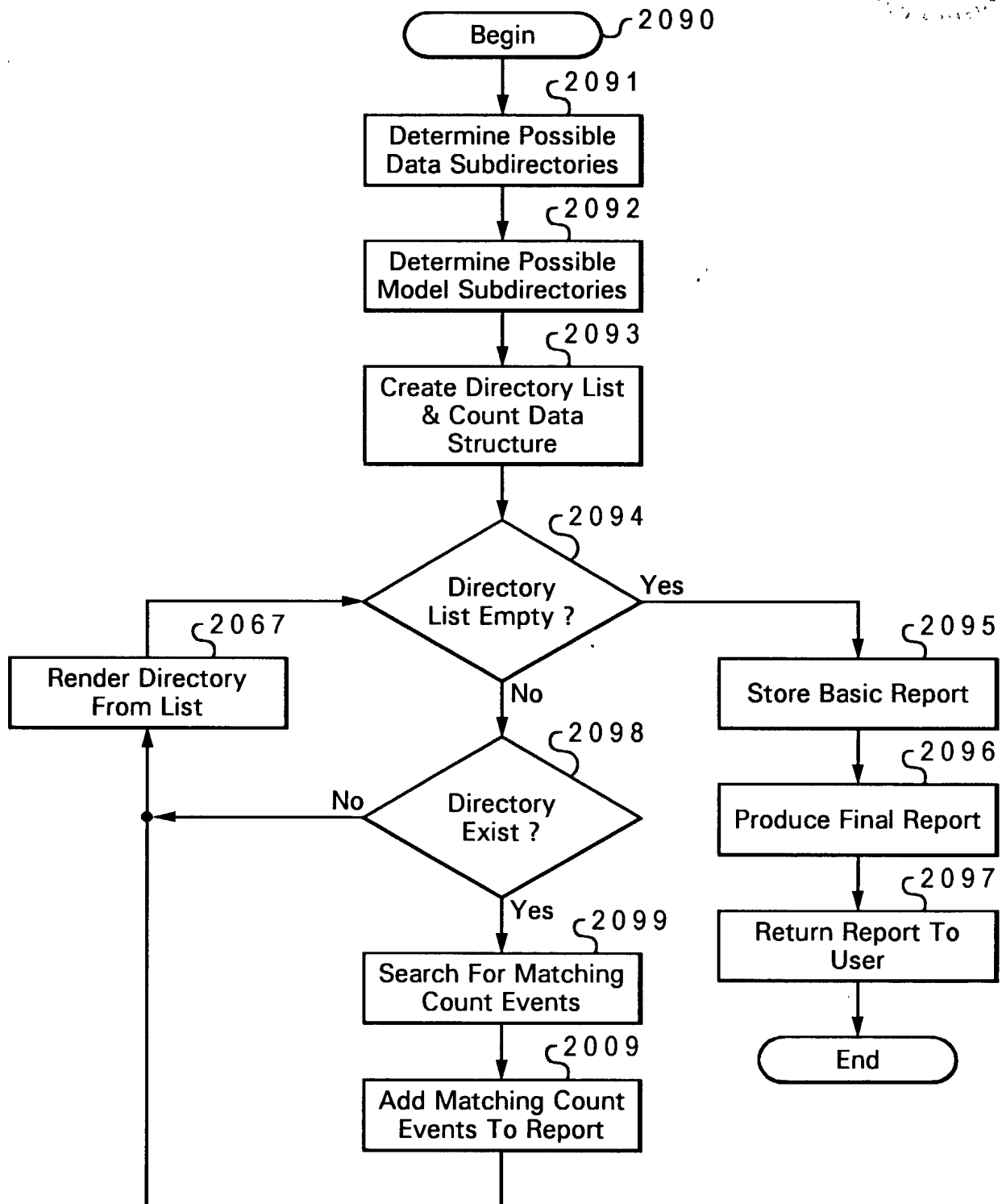
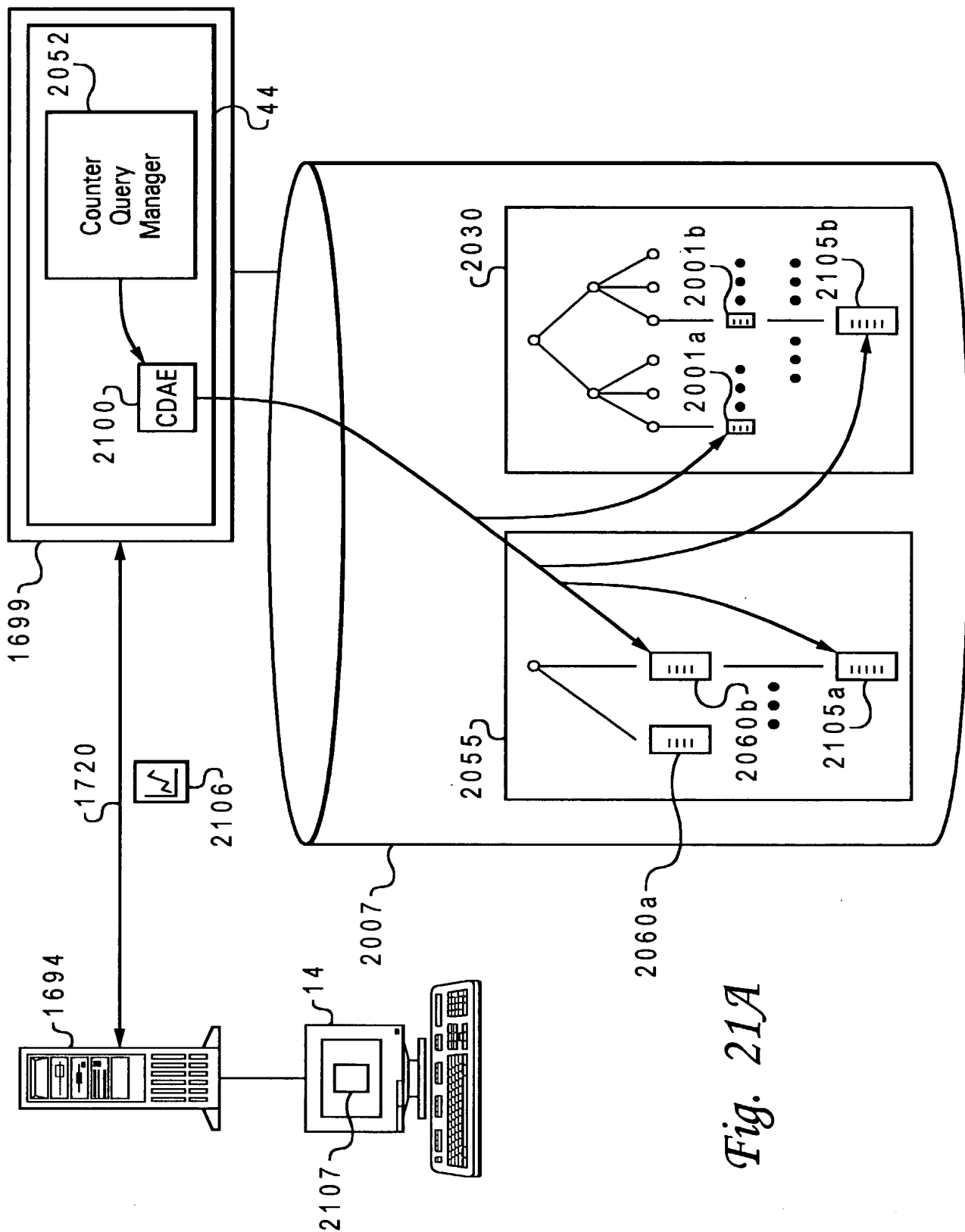


Fig. 20I



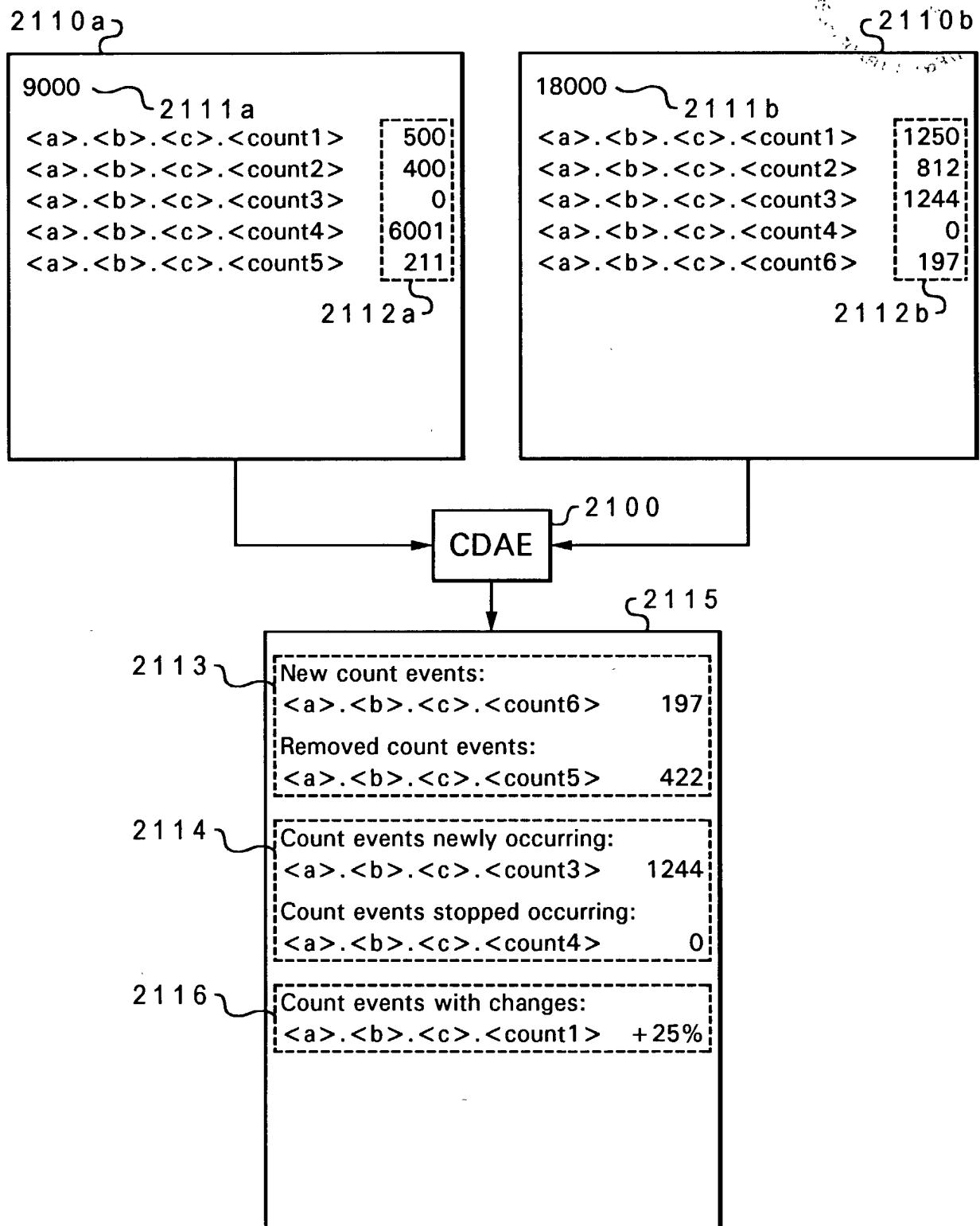


Fig. 21B

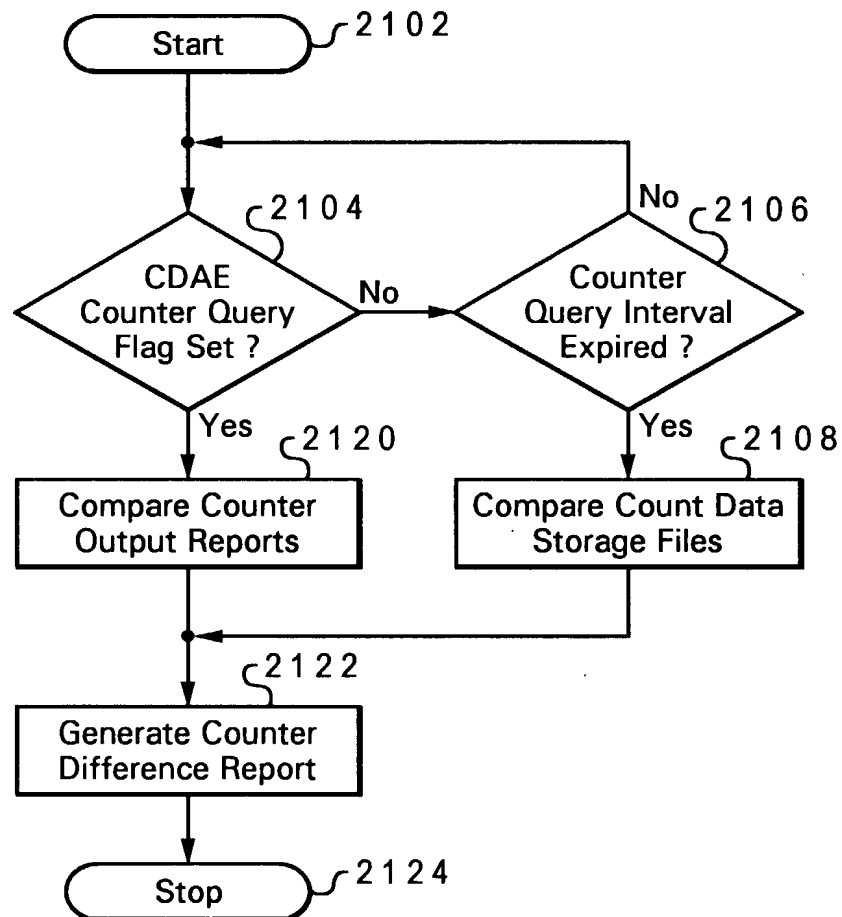
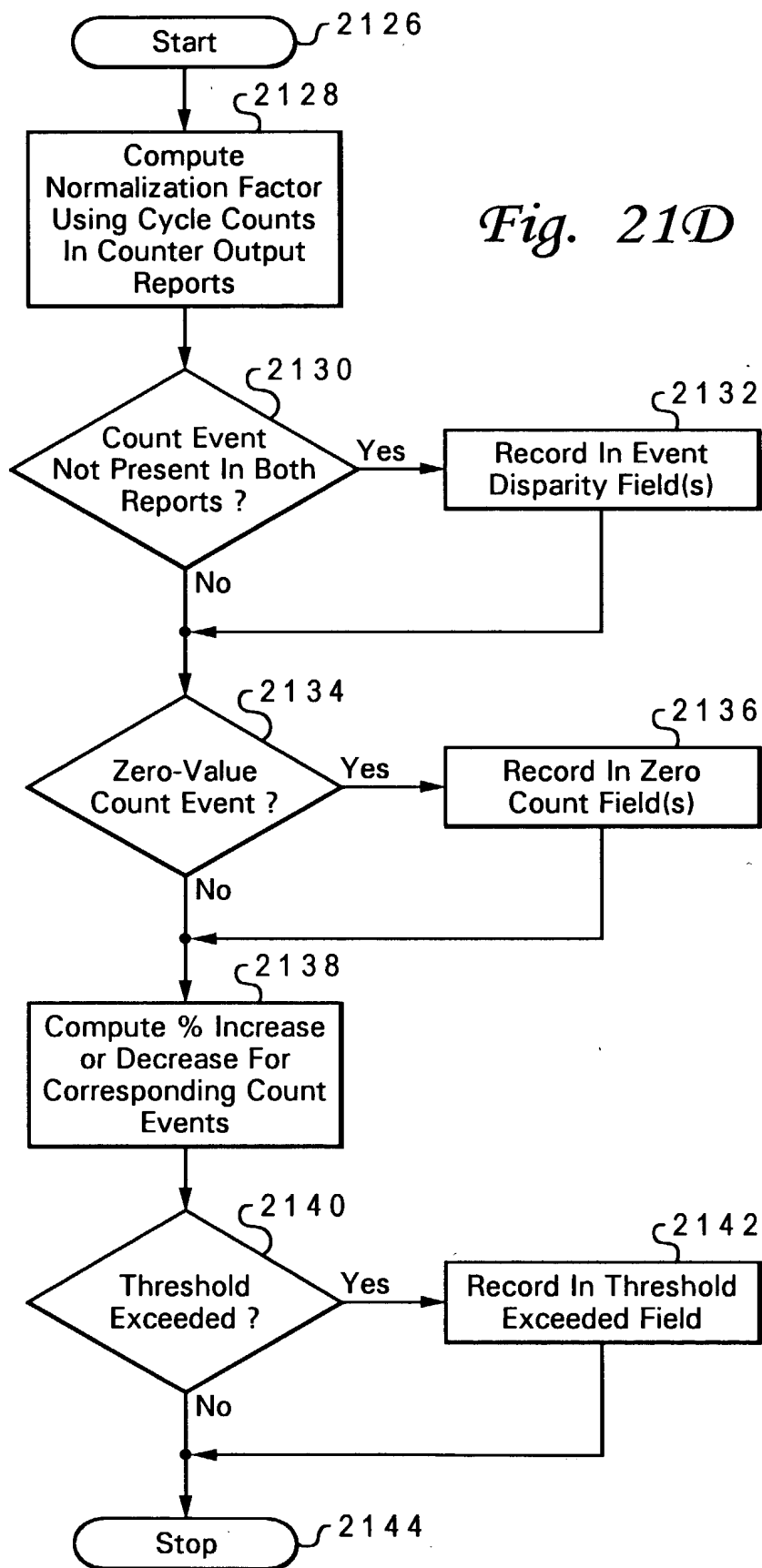


Fig. 21C

Fig. 21D



A circular logo for the American Society of Human Genetics (ASHG). The outer ring contains the text "AMERICAN SOCIETY OF HUMAN GENETICS" at the top and "1964" at the bottom. The center features a stylized graphic of a DNA double helix.



Fig. 22A

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Fig. 22B

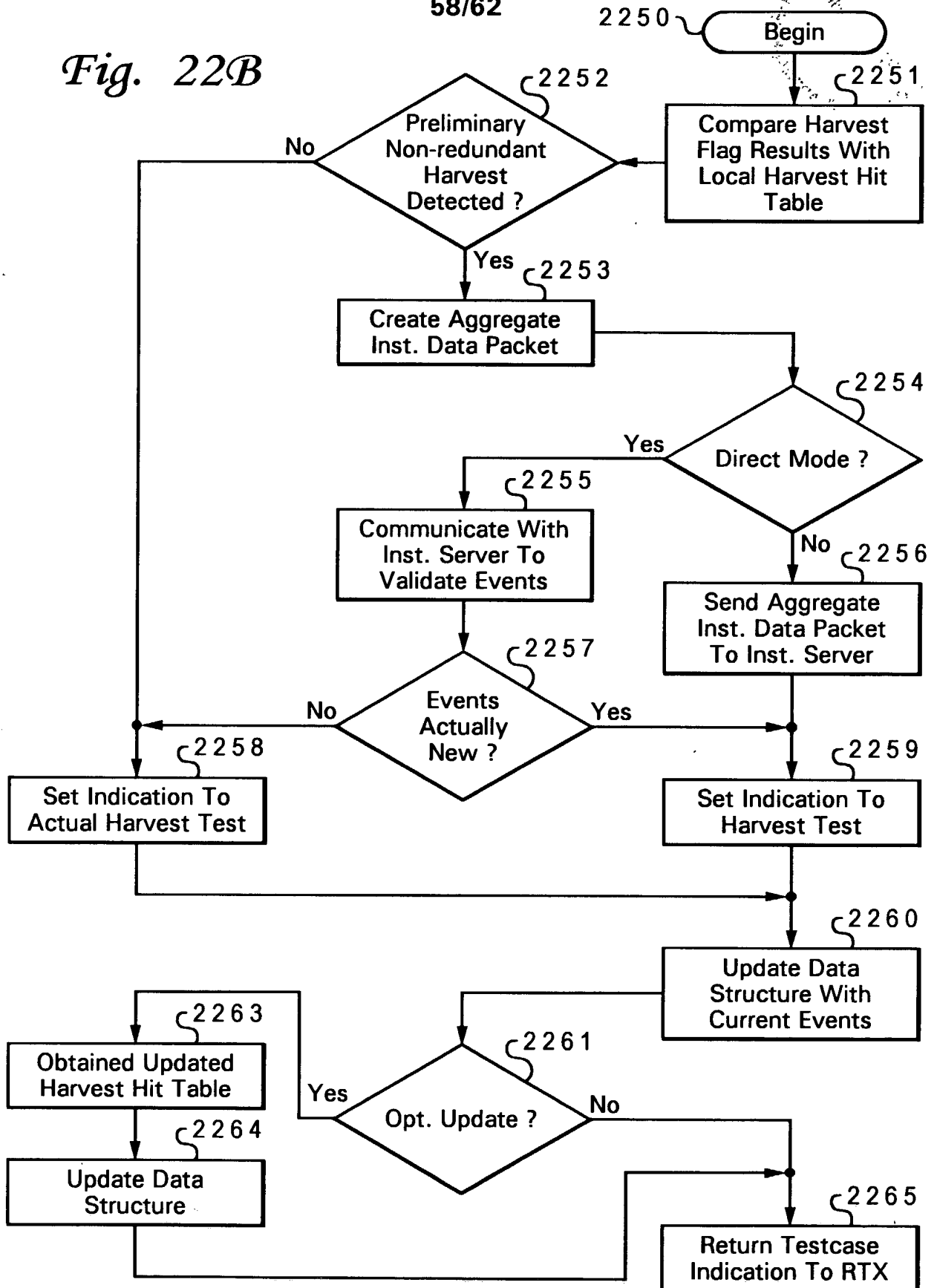
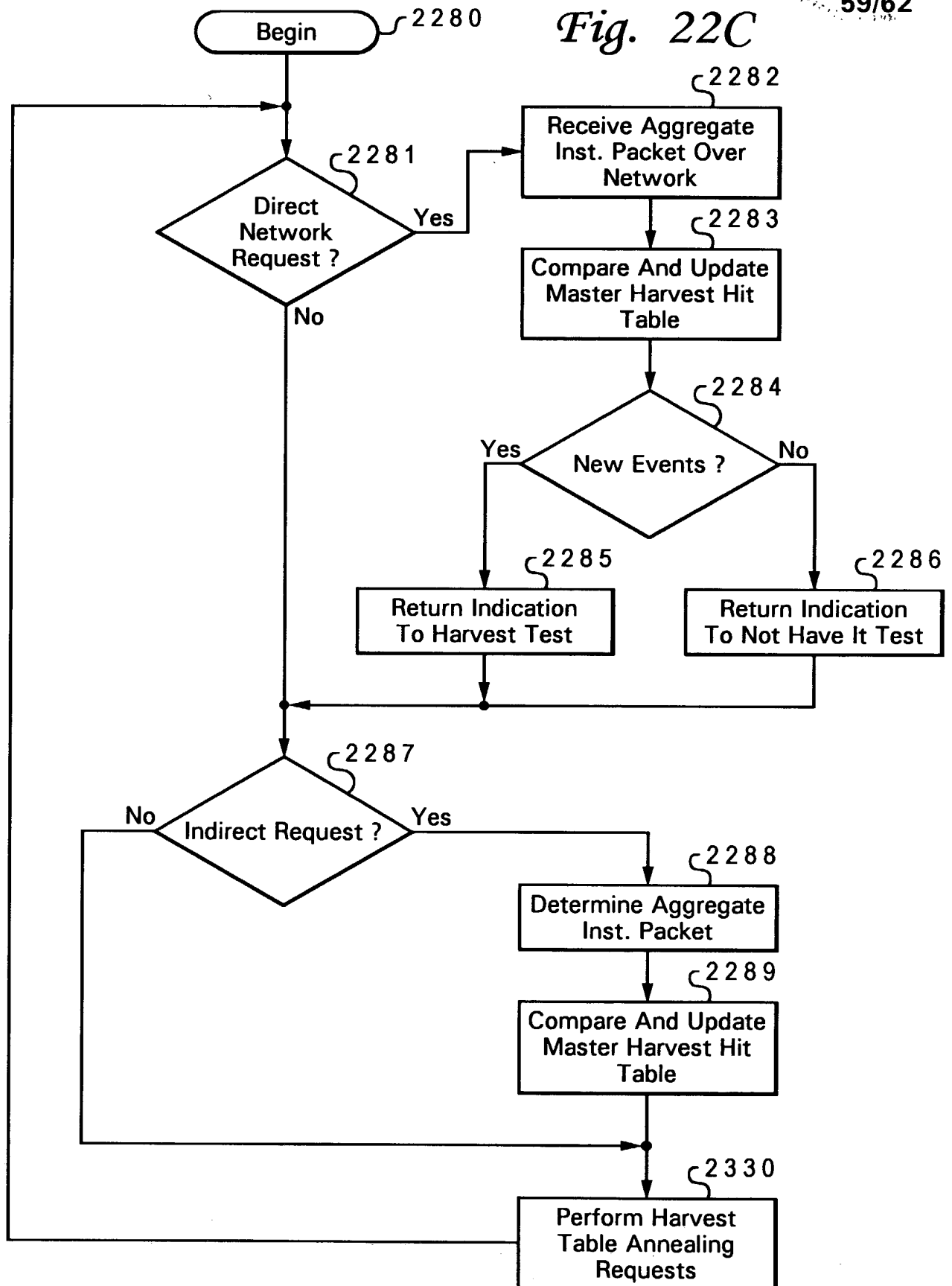


Fig. 22C



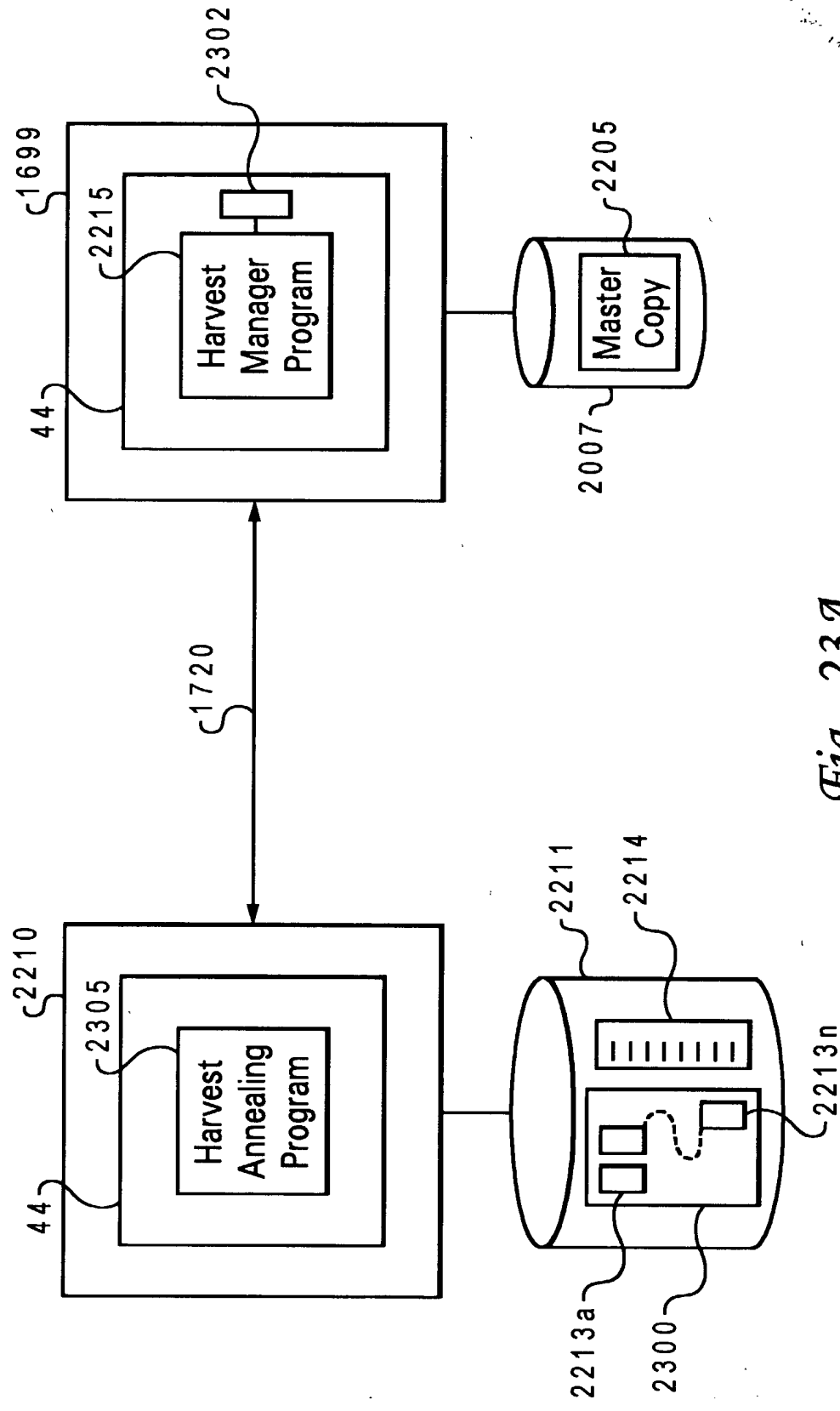


Fig. 23A

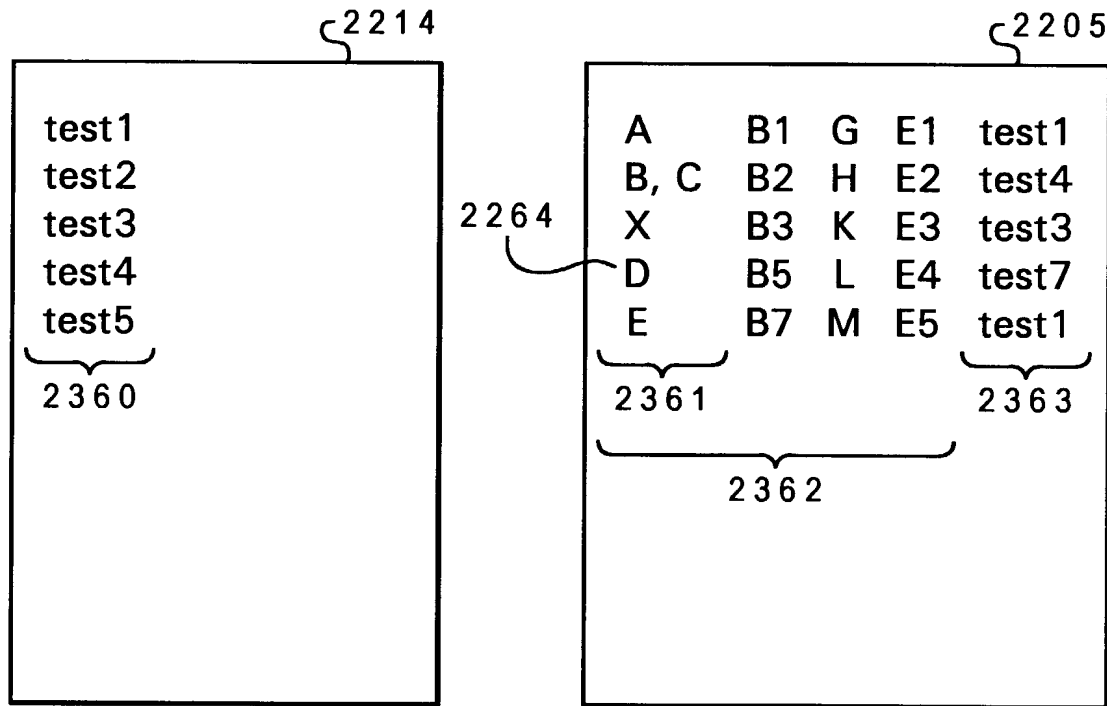


Fig. 23B

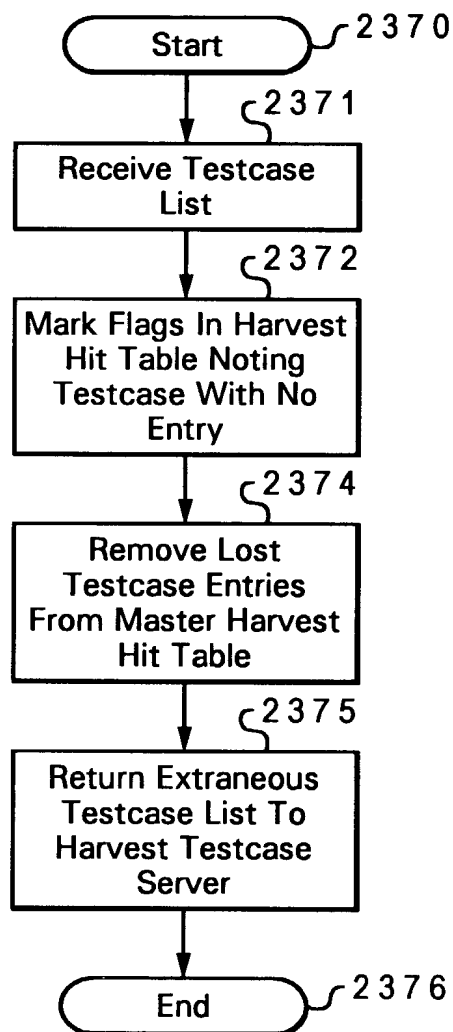


Fig. 23C